CORPORATE OVERVIEW

ENABLING NEXT-GEN SOLUTIONS

Silicon | Systems | Software | Product Engineering

OVERVIEW

Established in **1999**, with **25+ years** of Expertise.

Development Centers Across 5 locations | **USA** | **INDIA**

1300+ Employees: **900+** Semiconductor | **400+** Software Development

400+ Tape-outs From the Leading Foundries

Global Headquarters

Subsidiary / Branch Office

"WE ARE ONE OF THE VERSATILE ORGANIZATIONS WITH SOLUTIONS & SERVICES FOR ALMOST EVERY INDUSTRY" - CEO

OUR CAPABILITIES

SEMICONDUCTORS	*Semiconductor IP*	*Semiconductor Design*	*Turn-key ASIC*
SYSTEMS, SOFTWARE AND PRODUCT ENGINEERING SERVICES	*Systems Design*	*System Software Design*	*Product Engineering*

ISO 9001:2015 certification for SoC Design, Development, Assembly, Supply & Services of Semiconductors, Software, Systems

SEMICONDUCTOR CAPABILITIES

- DIGITAL IP
- VERIFICATION IP
- SERDES IP
- ADC/DAC IP
- PLL IP
- RTL DESIGN & VERIFICATION
- ANALOG LAYOUT
- PHYSICAL DESIGN
- RTL TO VOLUME PRODUCTION
- WORKING RELATIONSHIP WITH LEADING FABS
- SUCCESSFUL TRACK RECORD

ISO 9001:2015 certification for SoC Design, Development, Assembly, Supply & Services of Semiconductors, Software, Systems

SYSTEMS, SOFTWARE AND PRODUCT ENGINEERING CAPABILITIES

- HIGH SPEED PRODUCT & SYSTEM DESIGN
- PLATFORM DESIGNS WITH FPGA, SOC & ASIC
- DFM / DFA, & EMS
- PLATFORM BRING-UP & VALIDATION
- OS PORTING & BOARD SUPPORT PACKAGE
- ASIC DEVICE DRIVERS
- SOFTWARE INTEGRATION
- SOFTWARE TESTING
- SOFTWARE MAINTENANCE/ SUPPORT
- PLATFORM ENGINEERING
- AI ENGINEERING
- MULTIMEDIA ENGINEERING
- SYSTEM ENGINEERING
- QUALITY ENGINEERING
- DIGITAL & NETWORK ENGINEERING

KEY PARTNERSHIPS & ALLIANCES

FPGA DESIGN PARTNER	ADAPTIVE COMPUTING PARTNER	SENSAI MEMBER
FPGA Microchip Design Partner	AMD Xilinx	Lattice Semiconductor

BUILD PARTNER	DCA PARTNER	RISC-V PARTNER
Siemens	TSMC	tenstorrent

OUR BUSINESS VALUE PROPOSITION

- Silicon, Systems, Software & Product Engineering under single roof
- Replicated success over 25+ years with long term customer retention
- Continuous growth in relationship with leading semiconductor firms, foundries & EDA players
- Stability, low attrition & continuous knowledge upgrade on latest tools/technology

Alignment with client business cycle

End-to-end ownership

Flexible Business Model

Collaborative Approach

SEMICONDUCTOR IP

MIXED SIGNAL IP AND RELATED SERVICES

IP

Mixed-Signal IP

Standards Based IP

- PCIE Gen1/2/3 PHY
- SATA I/2 PHY
- XAUI PHY
- CEI-6G-SR-PHY
- SerialLite PHY & PCS
- ARM HSSTP PHY & Link
- PCIE Gen4 PHY (In Lab)

Analog IP

- ADC, LVDS I/O, PLL

Customer Specific:

- Custom SerDes for automobile / ADC / other applications

CUSTOMIZE

- MosChip Technologies offers customization to other Foundries/nodes and emerging standards

Porting to other foundries

- TSMC, Global, Tower, Samsung, Intel
- 180nm, 130nm, 55nm 40nm, 28nm, 22nm, 16FF, 14FF, 7FF, 6FF, 4FF, 5FF, 3FF

- Design services for customization / porting of customer's own technology

INTEGRATE

- Complete integration services of MosChip IP into customer's SOCs. In addition, provides design services in the following:
- Synthesis
- DFT
- Place & Route
- Analog/Mixed Signal Design
- Analog Layout

ANALOG IP CUSTOMIZATION SERVICES

Nodes		
TSMC	SAMSUNG	GLOBAL FOUNDRY
FinFET 3nm, 5nm, 6nm and 7nm	4nm	12LP
12FFC	5nm	14FF
28nm HPC, HPC+	12nm	22 FDX
40LP, 180nm		40nm, 55nm

CUSTOMER PROJECTS	INTERNAL PLATFORMS
DISPLAY PORT/HDMI SerDes (10G)	Long Range SerDes (16G)
Multi-Protocol SerDes (6.4G)	Short Range SerDes (10G)
DDR4, GDDR5 PHY	ARM HSSTP PHY (12.5G)
TOUCH SENSOR IMAGE SENSOR	ADC
Serial Lite SerDes (2.5G)	LVDS IO, PLL

Design Tools	Layout Tools	Other Tools
cadence	cadence, Mentor Graphics	MATLAB, SOS SYSTEMS, SystemVerilog

80+ Engineers

- Capable of providing Complex IP Porting solutions like Serdes, DDR
- Experience in working with Latest nodes in TSMC and Samsung
- Recognized TSMC Partner (TSMC DCA Partner)
- Adheres to strict IP Development Methodology
- Follows established CAD Flows and Methodology
- Adherence to ISO Standards, ISO9001:2015 Certified Company
- Professional Program Management and Status Updates

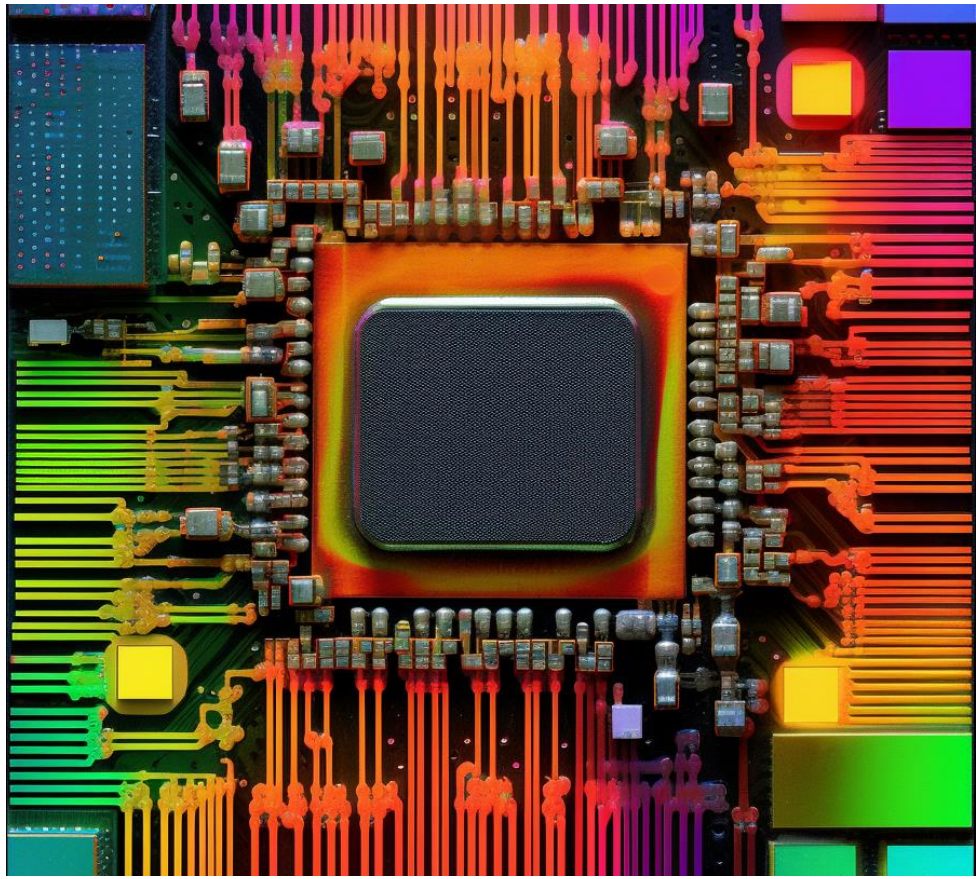
MOSCHIP SERDES IP

[Phy product standards' overview]

Name	Standards	PCS	Data Rate per Lane (Gbps)	Comments
PCIe Gen 1	PCIe 1.1	PIPE	2.5	• Endpoint or Root Complex • PIPE includes skip insertion, deletion • PCIe power savings modes
PCIe Gen 2	PCIe 1.1	PIPE	2.5	• Endpoint or Root Complex • PIPE includes skip insertion, deletion • PCIe power savings modes • Port bifurcation support
	PCIe 2.1	PIPE	5.0	
PCIe Gen 3	PCIe 3.1/2.1/1.1	Partners	8.0	• Endpoint or Root Complex • PCIe standard multi-lane interface
XAUI	XAUI, CX4, KX4	Customer	2.4 - 3.2 / 1.2 - 1.6	• Generic backplane uses
CEI-6	CEI-6, XAUI, CX4, KX4	Customer	4.8 - 6.4 / 2.4 - 3.2 / 1.2 - 1.6	• Generic backplane uses
SATA I/II/III	SATA I/II	SATA	1.5/3.0	• Advanced frequency offset (PPM) compensation for +0 / -0.5% SSC
	SATA III	SATA	6.0	
Switchable	Multiple	Multiple	Multiple	• Switchable between 2 or 3 standards • Separate interface for each standard
ARM HSSTP	HSSTP 6.0	Aurora Link	6.25 / 12.5	• ARM HSSTP PHY along with Link Layer as a single macro
PCIe Gen4	PCIe 4.0	Partners	16	• Test silicon functional and in CHAR/Debug
Seriallite PHY	IEEE149.1	PCS	3.125	• chip2chip, board2board, shelf2shelf or backplane
10/100/1000 Ethernet	IEEE802.3	PCS	1	• AFE Block in development
USR/VSR/SR		PCS	10	• Chip to Chip SerDes. In Development

MOSCHIP DIGITAL IP

USB	SECURITY	ENCRYPTION
• Host Controller • Device Controller • Retimer • Dual-Role-Device	• Secure Hash Algorithms (SHA1, SHA2, SHA3) • Reed-Solomon based FEC • Reed-Solomon based Erasure (Static & Dynamic)	• Advanced Encryption Standard (AES 128, AES 256) • XTS-AES



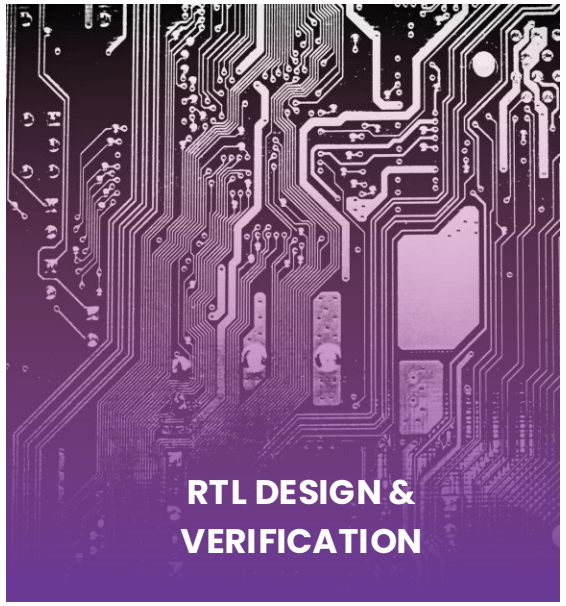
Best in class performance

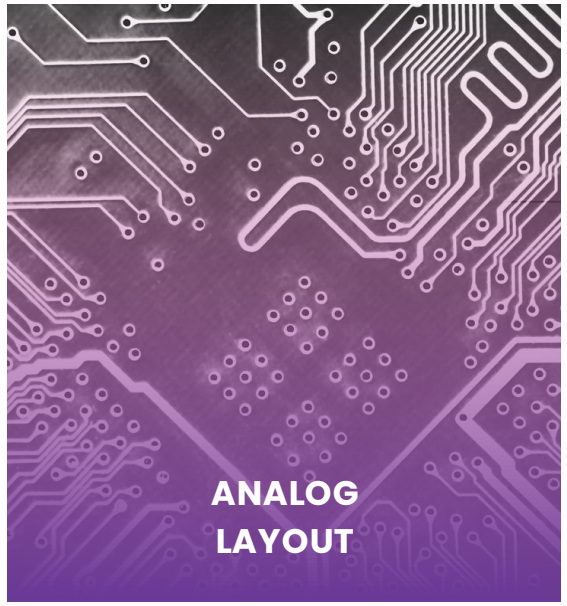
Up to 20% Better throughput

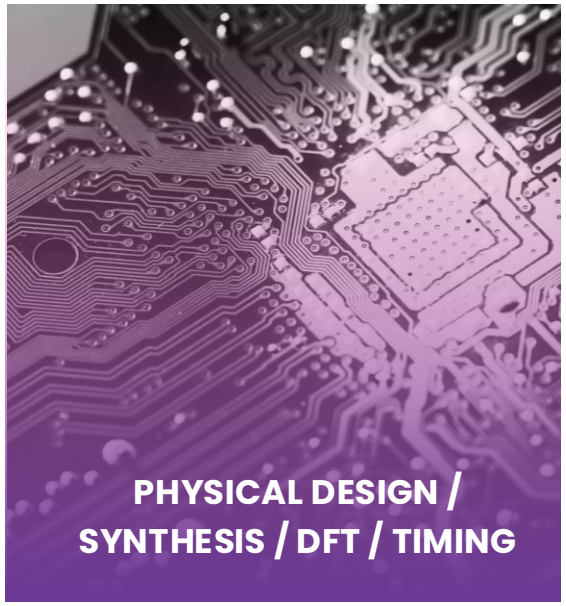
Platform Independent

SEMICONDUCTOR DESIGN SERVICES

OVERVIEW OF SEMICONDUCTOR GROUP







- Achieved "**first-pass silicon success**" across **400+** tape-outs
- Expertise ranging from **500nm** to the latest **3/5/6/7/10/14/16 nm FinFET & SOI process nodes**
- Very strong **RTL Design, Design Verification, Physical Design, Analog Design, and Analog Layout** team with over 15 years of average experience in the senior team
- Engaged in complex chip designs extending to **100+ million gates**
- Highest level of training & experience on state-of-the-art technologies
- Design Houses in **Hyderabad, Bengaluru, Ahmedabad, Pune** and **Santa Clara, USA**

900+ VLSI Engineers

400+ Tape-outs with 100% First-Pass Silicon Success

Engagement Model
ODC | T&M | Turnkey

RTL DESIGN & VERIFICATION SERVICES

18+
AVG.EXP. OF LEADERSHIP

100+
TAPE-OUTS

200+
ENGINEERS

RTL DESIGN & VERIFICATION

RTL Design

- RTL Front-end Design & Integration
- Micro-architecture Design
- Synthesis & Optimization
- Low power and GLS
- IP/VIP Development, 3rd party IP/VIP& SoC integration

Verification

- SV/UVM Expertise
- Assertion based Verification
- Constrained Random & Coverage-driven Verification
- IP/SoC level Verification
- IP to SoC Verification Sign-off

Turnkey

- Concept to Deployment
- IP to SoC Design & Prototyping
- Architecture, Coding, Testing, Release & Support
- Functional Verification

Processors

arm

RISC-V

tensilica

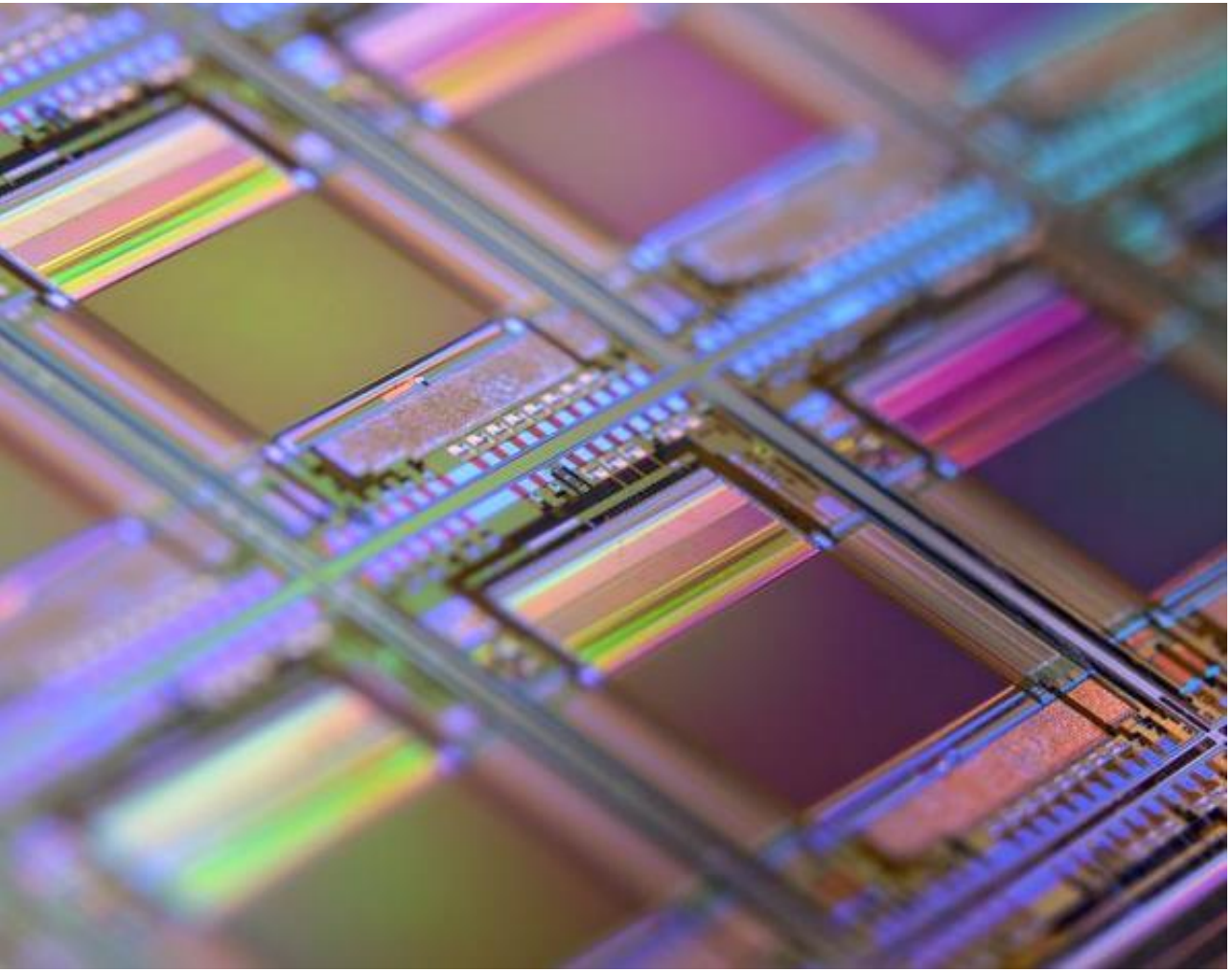
mali Visual Computing by ARM

Highlights

- Digital IPs/Subsystem – GCC, and Arite core
- Mixed signaling IPs – Tejas, Brain beats and Borealis
- Turnkey project – Matrix SoC

TECHNOLOGY EXPERTISE

IP Interfaces / Protocols	Verification Tools	Languages & Methodology	Scripts	Prototype Platforms
Ethernet HDMI | SATA SAS | CAN AXI/APB xHCI | PIPE UTMI+ULPI SPI | I2C Interlaken MIPI | DP	Questa | Incisive VCS | Jasper QuestaFormal Xcellium Simvision Visualizer Codelink Verdi Formality FormalPro QuestaSLEC Conformal	SystemVerilog UVM	python Perl .SH	intel ALTERA now part of Intel cadence XILINX LATTICE SEMICONDUCTOR



ANALOG LAYOUT SERVICES

18+
AVG.EXP. OF LEADERSHIP

150+
TAPE-OUTS

250+
ENGINEERS

ANALOG LAYOUT SERVICES

Technologies

- TSMC - N3E | N3P | 5FF | 6FF | 7FF | 12FF | 16FF
- TSMC - 22nm, 28nm, 180nm
- SAMSUNG - 3nm, 4nm, 5nm, 7nm
- GF - 14nm, 12nm, 22nm, 40nm, 55nm, 65nm

Expertise

- High Speed Serdes up to 112Gbps – Very Short Reach or Extra Short Reach Serdes of 112Gbps data rate, PCIe6 Gen Protocols
- Power Management Layouts – LDO, BGR, SMPS, Bias blocks, Buck Boost converters, etc.
- I/O cells – GPIOs, LVDS, DDR Ios and GDDR IOs
- Data Converters – ADC, DAC with different architectures (Pipeline, SAR ADC, Flash ADC, Current steering DAC and R-2R ladder DAC)
- RF Layouts
- Memory Layouts – Register files, Dense RAM, Cache Memory, CAM Memory
- Clock Generators – Phase Locked Loop, Delay Locked Loop

Unveiling

- Ready to Tape-out the Chip in 3nm
- TSMC 22nm Ultra Low Leakage (ULL) AIoT Edge AI SoC for NTU, ASTAR & EMass.ai [RTL-Silicon]

Highlights

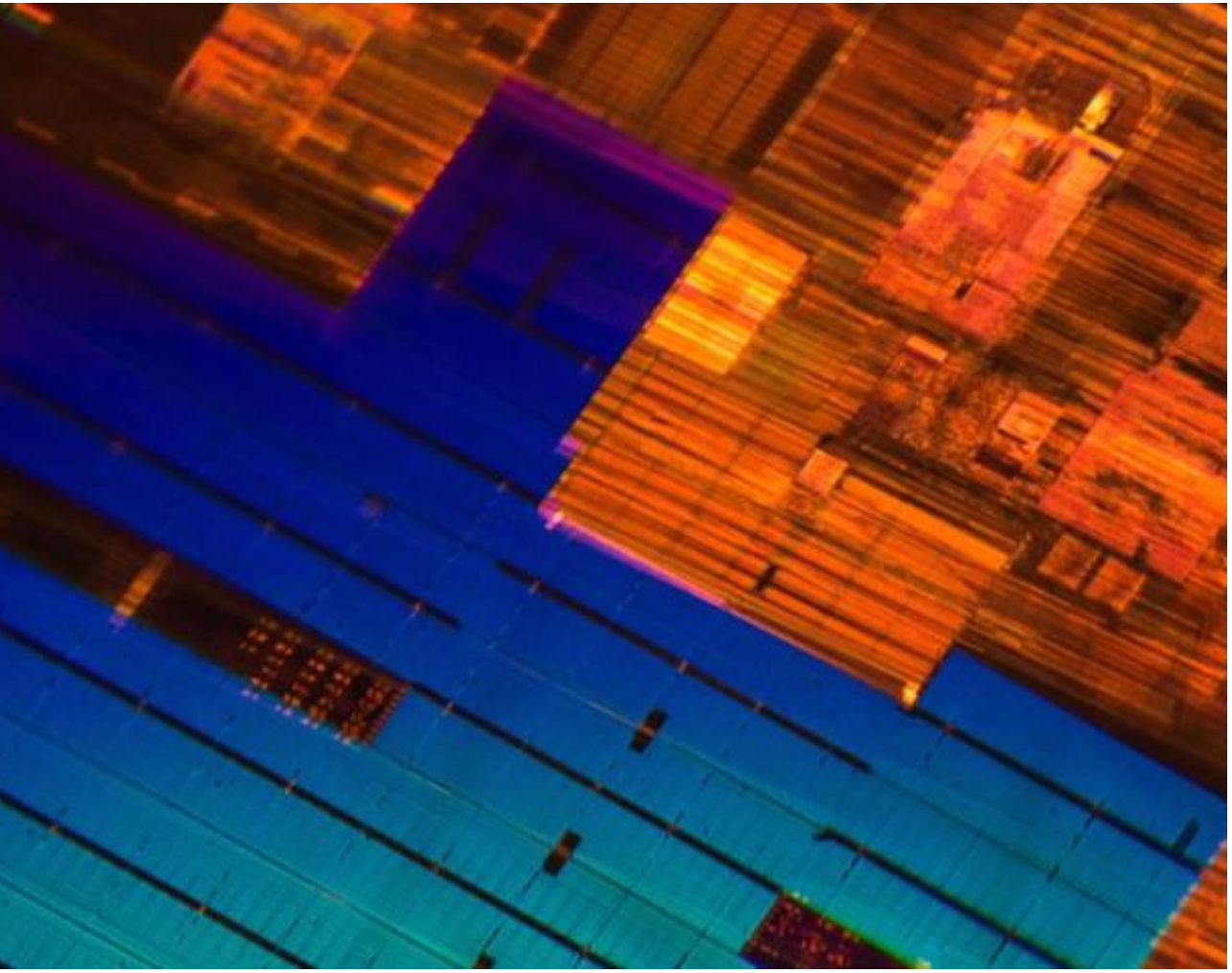
- SerDes - Up-to 112GBPS
- SerDes - PCIe5 & PCIe4 with Multiprotocol support
- SerDes - Up-to 112GBPS

Tools

cadence
Mentor Graphics
Ansys
SYNOPSYS

ANALOG LAYOUT – IP DETAILS

PRODUCT	TECHNOLOGY	SPECIFICATION	APPLICATION
XSR SerDes	TSMC N5	112 Gbps	Networking/Servers
PCIe Gen6	TSMC N5	64 Gbps	Networking / Servers
DDRIO	TSMC N3	4.8 Gbps - 5.6 Gbps	Memory Applications
DDRIO	TSMC 5G	4.8 Gbps - 5.6 Gbps	Memory Applications
DDRIO	Samsung 5nm	4.8 Gbps - 5.6 Gbps	Memory Applications
Graphical DDR	TSMC 12FFC	12 Gbps	Memory Applications
PMU / PMW Controllers	TSMC180		Laptop / Servers
High Precision Oscillators	TSMC N55	Speed of 5Ghz	Aerospace, Defense, Automotive, Electronics, Mobile & IoT
Clock Generator	TSMC N3	Speed of 5Ghz	Processors
Smart Electrical Meter IC	TSMC 180	45-55Hz, 1 Phase / 3 Phase	Electric Measuring Applications



PHYSICAL DESIGN SERVICES

20+
AVG.EXP. OF LEADERSHIP

150+
TAPE-OUTS

400+
ENGINEERS

PHYSICAL DESIGN SERVICES

EXPERTISE

- Block-Level Place & route
- Timing Closure & Static Timing Analysis
- Multiple Domain Clock-Tree Synthesis
- Physical Verification (DRC/ERC/LVS)
- EM-IR Drop Analysis, SI Closure
- Chip-Integration
- Logic Synthesis & Physical Synthesis
- Low Power Expertise – Clock Gating, Multi-Vt, Voltage Islands, Power Gating

FLIP-CHIP EXPERTISE

- O-ring design
- Bump Assignment work with Package team and Finalize
- Customer Designed Bump/RDL integration to chip level
- RDL Design and Routing
- Help Customers to decide Metal Stack
- Bumps and Package

Leadership History

ttm Time To Market Inc.
GigaCom
FIRSTPASS Committed to customer success
MOSCHIP

Foundries

tsmc
GlobalFoundries
SAMSUNG SEMICONDUCTORS
Tower Semiconductor

Tools

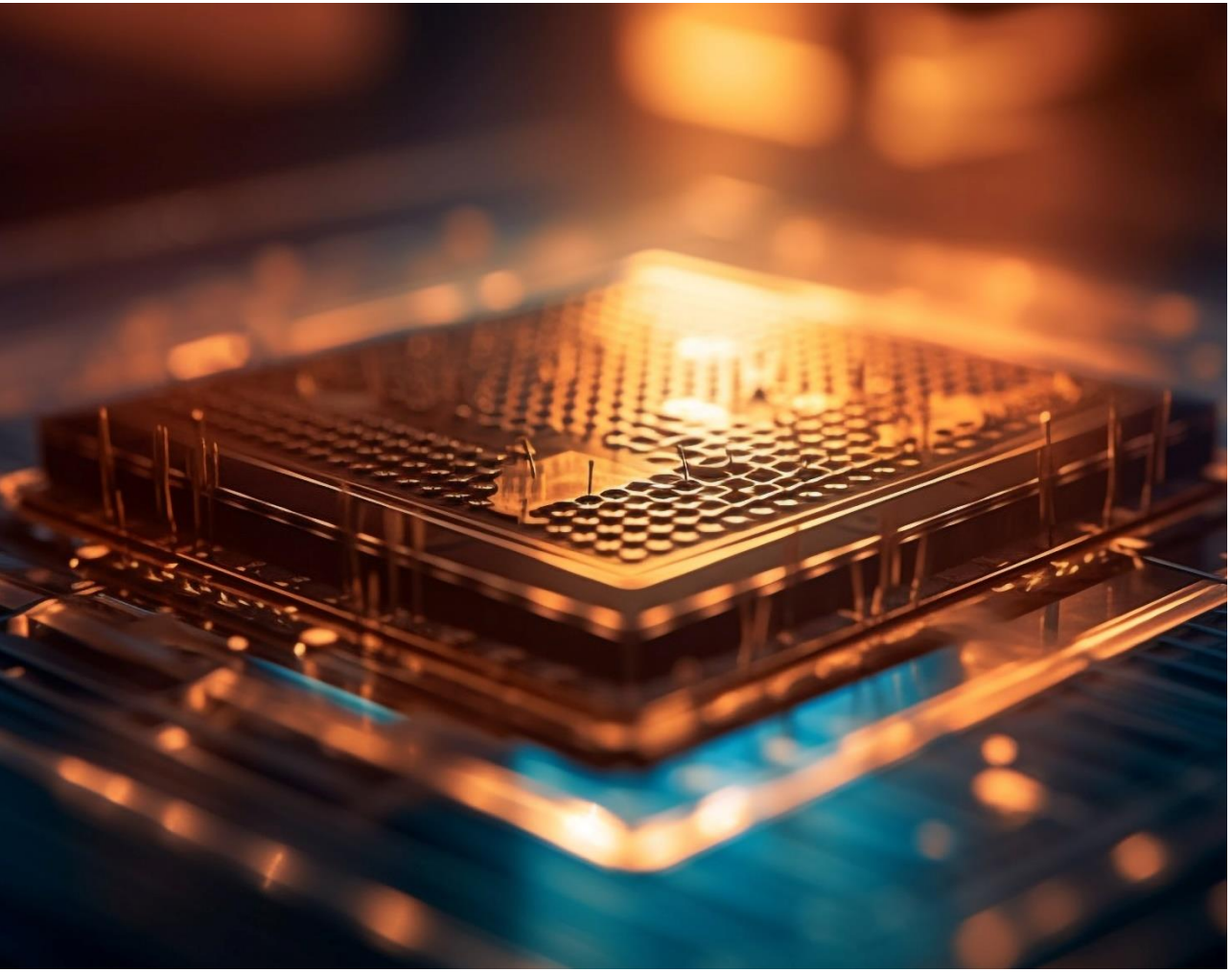
cadence
SIEMENS
SYNOPSYS
Mentor Graphics

Highlights

- Full-Chip Integration | Floor-Plan | Analog Integration | IP-Integration
- Full-Chip Pin-Assignment & Budgeting | Power-Grid Design & Analysis
- Clock-Design | timing Closure | Physical Verification & EM-IR
- DDR-Integration using new generation timing libraries (LVF)

SUMMARY OF PD PROJECTS

PROCESS	APPLICATION	DESIGN FEATURES	TEAM SIZE PD ENGINEERS	FLOW	DURATION MONTHS
TSMC 5nm	Client SoC	~ 75M gates, ~ 30 Blocks	15	Customer	12
TSMC 6nm	Client SoC	~ 190M gates, ~ 66 Blocks	35	Customer	12
TSMC 6nm	Client SoC	~ 70M gates, 20 Blocks	15	Customer	7
TSMC 6nm	GPU	~ 365M gates, ~ 100 Blocks	50	Customer	11
TSMC 7nm	GPU	~ 275Mgates, ~ 80 Blocks	44	Customer	12
TSMC 16nmFFP	Video Game	~ 22M gates, 25 Blocks	10	Customer	10
GF 14LLP	Graphics	~ 40M gates, 30 blocks	11	Customer	12
TSMC 28nm HPC+	Networking	~ 103M gates, 14 Blocks	12	MosChip	15
TSMC 40nm G	Networking	~ 12M gates, 8 Blocks	8	MosChip	7
GF 14nm HPP	Ethernet	~ 28M gates, 9 Blocks	6	MosChip	7
TSMC 28nm HPC+	GSP	~ 93M gates, 3 (Unique) Blocks	6	MosChip	12
Samsung 14nmLPP	GSP	~ 120M gates, 3 (Unique) Blocks	6	MosChip	12
TSMC 22nm ULL	Edge SoC	~ 2.2M gates, Flat Chip	3	MosChip	4



SEMICONDUCTOR TURNKEY ASIC

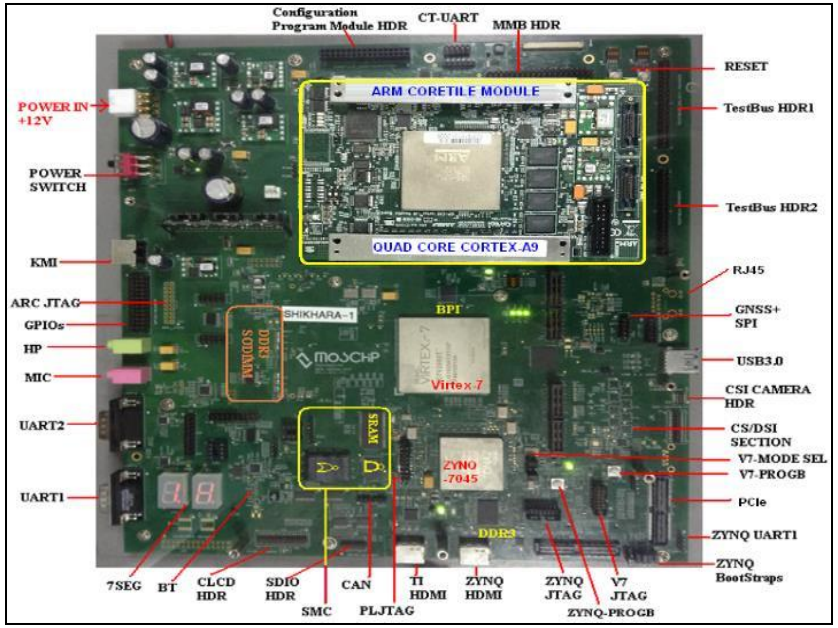
[RTL TO VOLUME PRODUCTION AND BRING-UP]

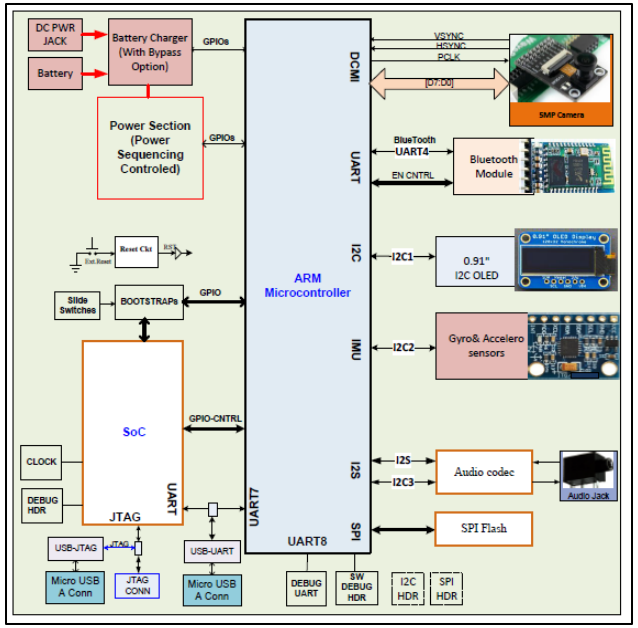
TURNKEY ASIC ECOSYSTEM PARTNERS

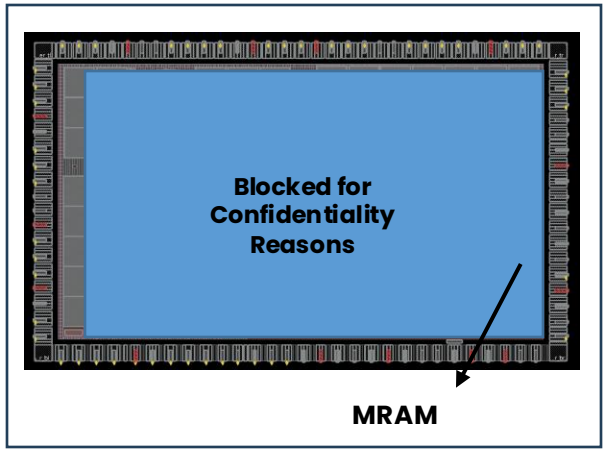
RTL to Volume Production

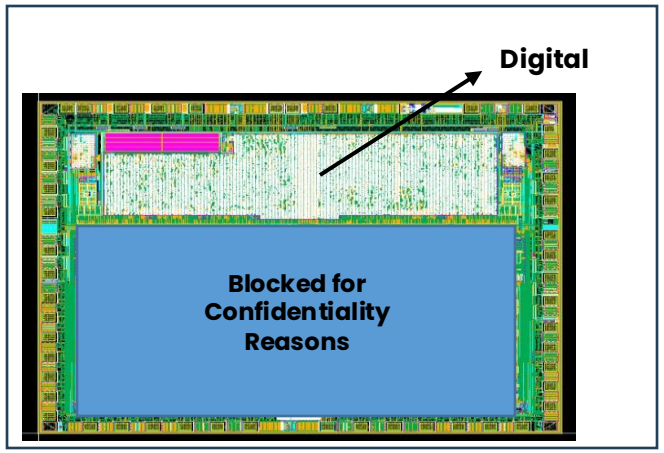
TURNKEY ASIC

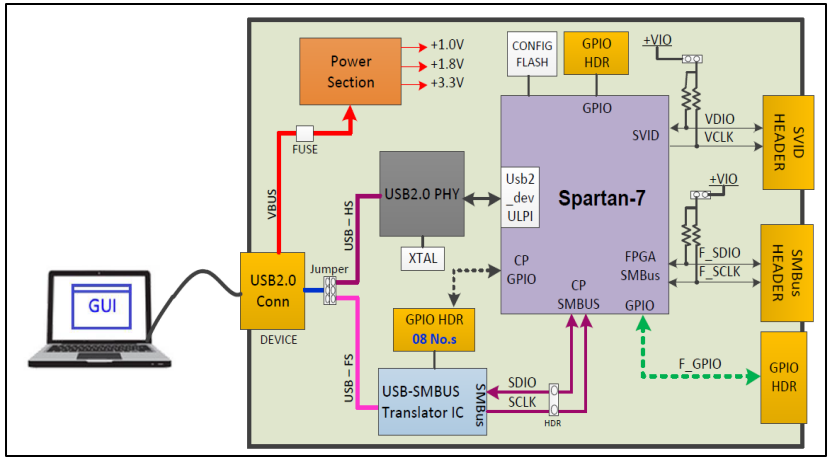
- Turnkey ASIC – Edge SoC
- Turnkey Mixed Signal ASIC – POWER IC
- Edge SoC Reference Platform & Bring-up
- Power IC - Debug Platform Development
- Turnkey ASIC – Matrix (Digital SoC)
- Matrix - FPGA Platform Pre-Silicon Validation
- Matrix – Reference Platform & BSP

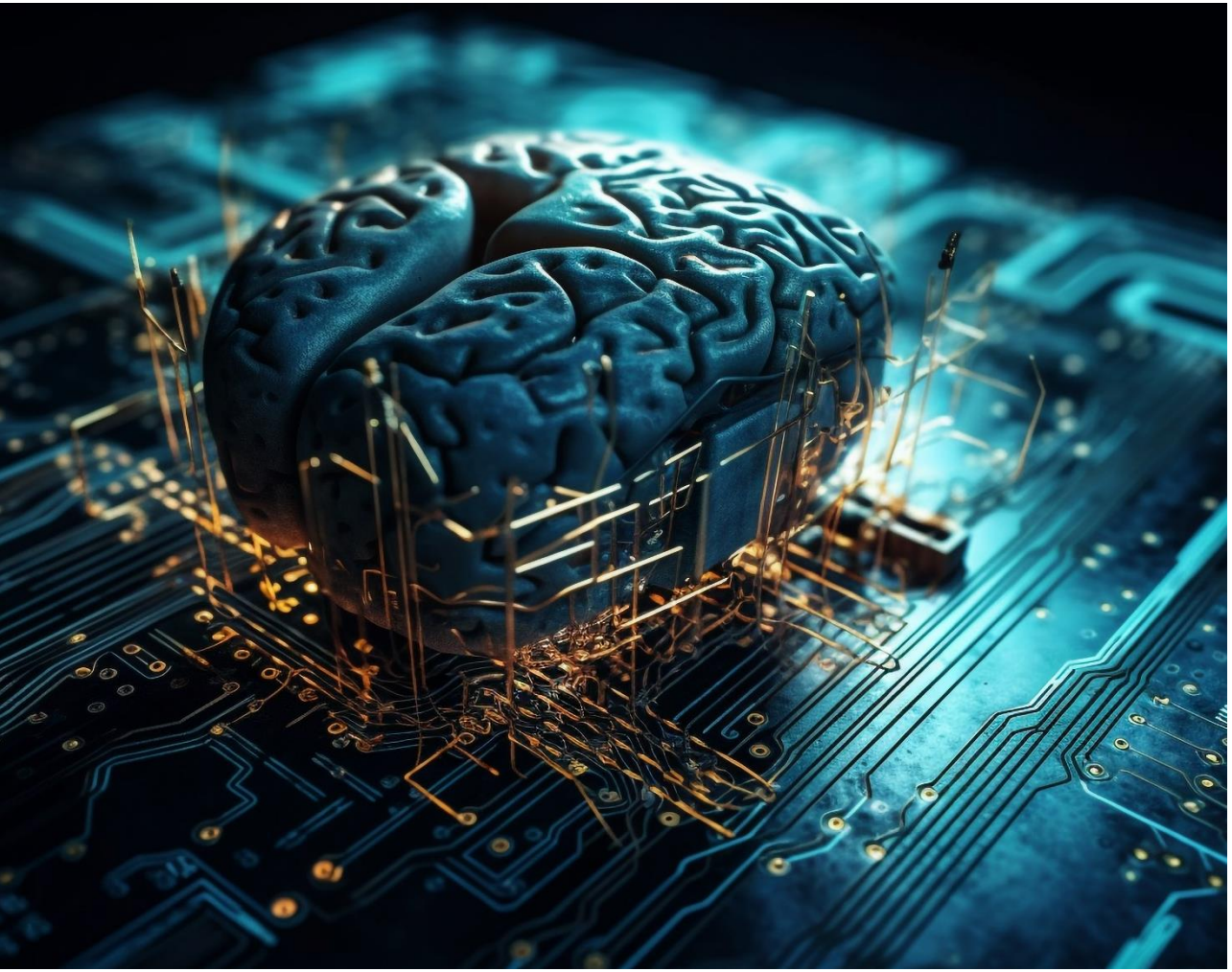








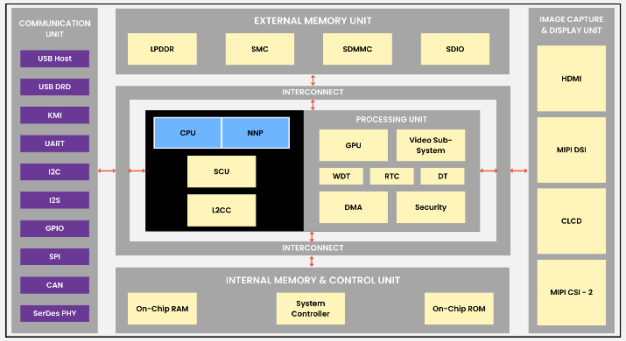




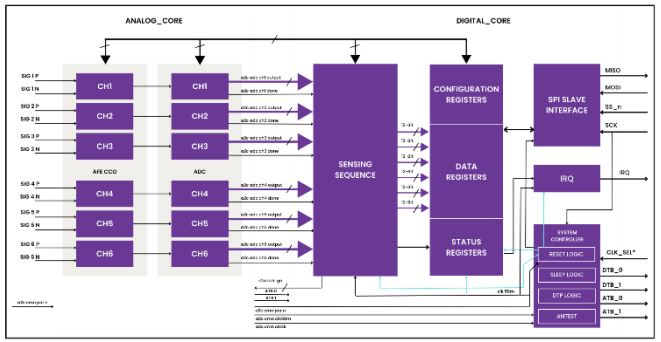
MOSCHIP ASIC PLATFORMS

MOSCHIP ASIC PLATFORMS

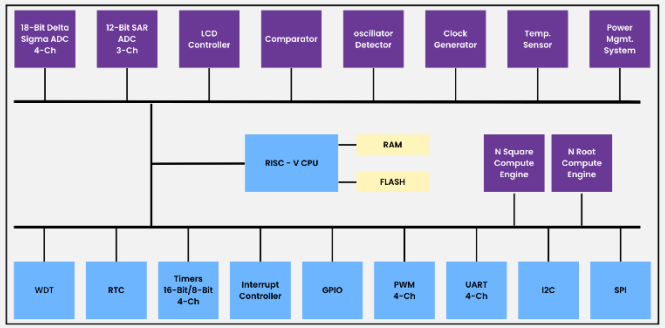
NNP BASED ASIC PLATFORM FOR EDGE AI



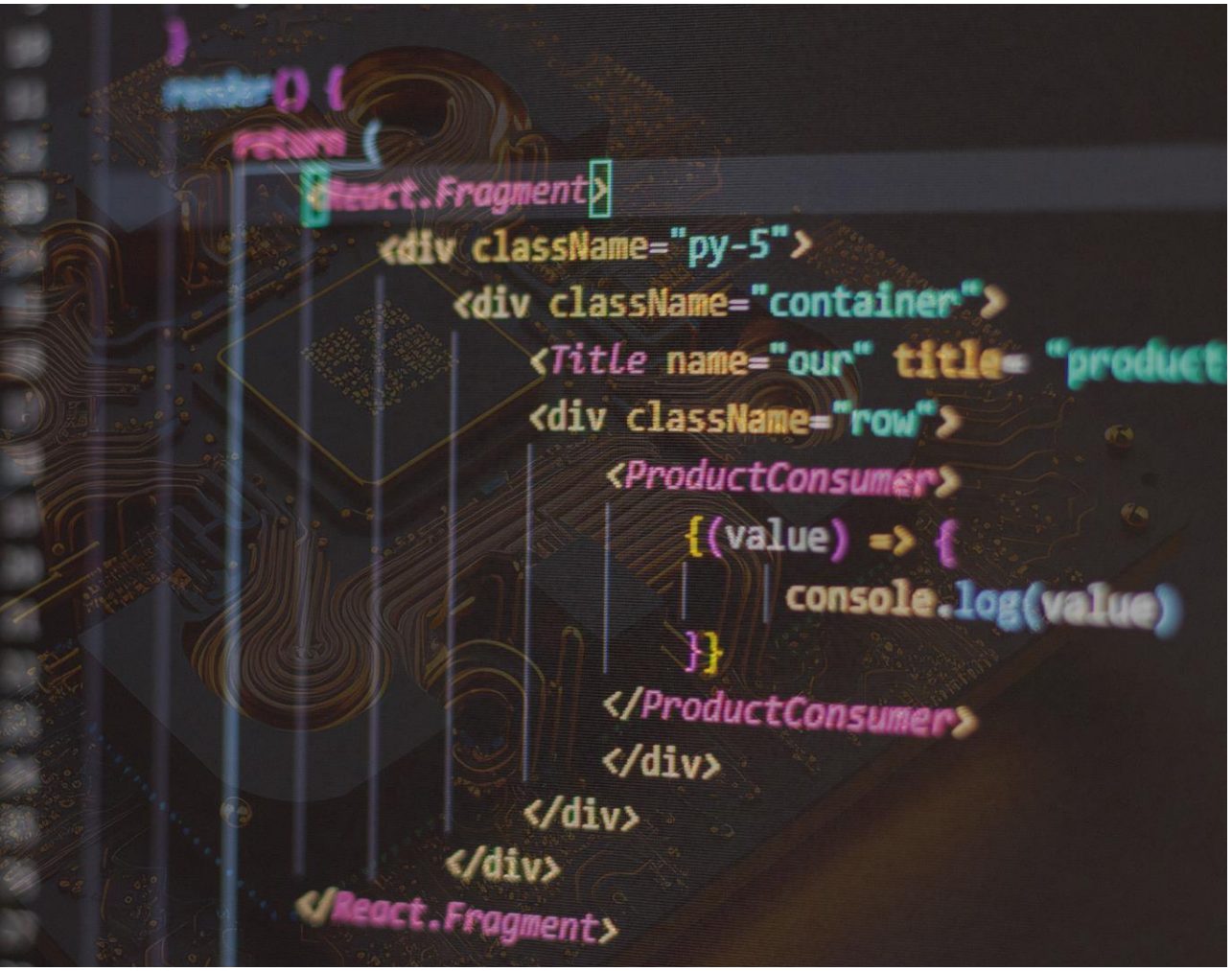
LOW FREQUENCY MONITORING ASIC PLATFORM FOR HEALTHCARE



RISC-V BASED ASIC PLATFORM FOR SMART METERS

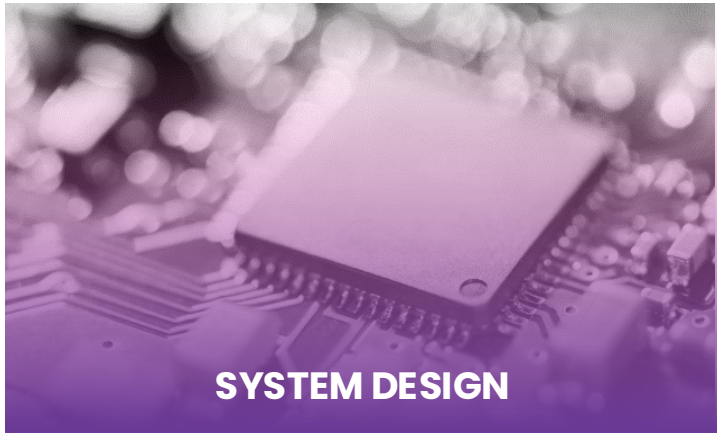


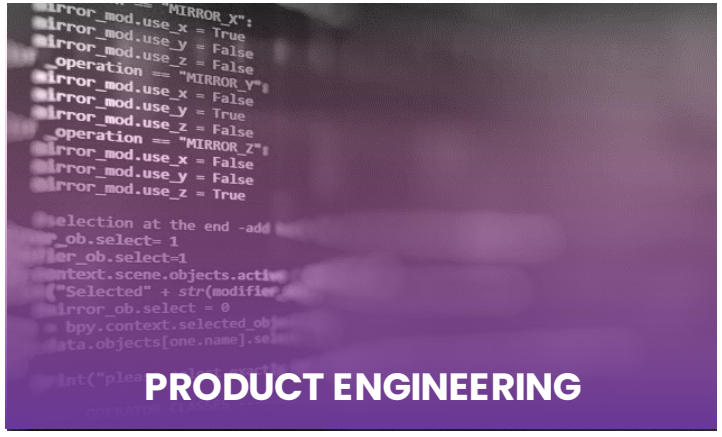
LEGENDS - Third Party | Partners | MosChip



SYSTEMS, SOFTWARE & PRODUCT ENGINEERING SERVICES

OVERVIEW OF EMBEDDED GROUP





- 23+ years of experience in Embedded Systems, Software and Product Engineering
- Enabling end-to-end solutions from concept to design and sustainability
- Skilled at building miniaturized, low-energy, high-accuracy secure portable solutions
- Empowering digital and product transformation for domains involving Medical, Storage, Computing, Multimedia, Automotive, Consumer, Defense and more
- Embedded expertise in Video, Audio, ML, and AI solution development along with Edge and Cloud deployment

400+ Engineers

500+ Projects

Experience of full Product Lifecycle

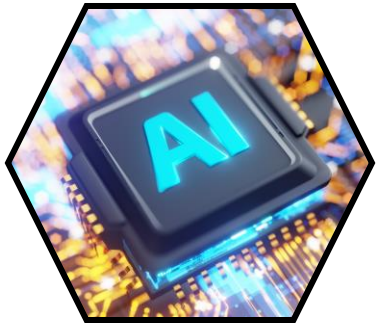
Engineering Partners for Indian Defence Labs

EMBEDDED SOFTWARE SERVICES

Platform & Systems Engineering

Multimedia Engineering

Digital Engineering



AI Engineering

Quality Engineering

Network Engineering

PLATFORM & SYSTEMS ENGINEERING

FPGA DESIGN	EMBEDDED SYSTEMS, SOFTWARE & PRODUCT DESIGN
• RTL Front-End Design & Integration • FPGA Software & Systems Bring-up • FPGA Acceleration Solutions • Interface & IP Integration • Reference Design	• Platform Enablement • Firmware & Driver Development • BSP & Board Bring-up • PCB Layout, OS Porting & Bootloader Optimization • Middleware Integration • Product Re-Engineering & Sustenance • Turn-key solutions with System/Product Design and Software Development • System validation, feature & benchmark testing • Customization, Maintenance, and Support • Formfactor Designs for Custom or COTS Enclosures

yocto PROJECT · Code Composer Studio · XILINX VITIS · LDRA · LATTICE sensAI · Auvid · LATTICE RADIANT · IAR Embedded Workbench · OpenWrt · PyCharm · Audacity

LATTICE sensAI · Linux · ANDROID · ARMmbed · VxWorks

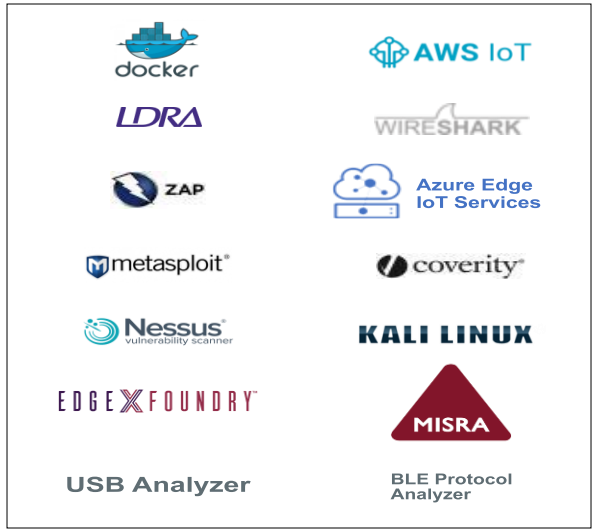
Custom Linux

docker · AWS IoT · LDRA · WIRESHARK · ZAP · Azure Edge IoT Services · metasploit · coverity · Nessus vulnerability scanner · KALI LINUX · EDGE X FOUNDRY · MISRA

USB Analyzer · BLE Protocol Analyzer

PLATFORM & SYSTEMS ENGINEERING

SECURITY	COMPLEX/HIGH SPEED SYSTEMS DESIGN
• Secure Platform Root-of- Trust (PRoT) • Fuzz & Penetration Testing • Edge to Cloud Security • Device & Data Security Lifecycle Management • Identity & Access Management	• System Architecture / Schematic Design • SI / PI / Thermal Sims • System Integration & Software Testing • Design updates with Version Control, Prototyping and Manufacturing



AI ENGINEERING

COMPUTER VISION	ML LIFECYCLE MANAGEMENT	COGNITIVE COMPUTING	AI/FPGA ACCELERATION SOLUTIONS
• Machine & Computer Vision Algorithms • Object Detection, Identification & Visual Perception • Image Capture & Optimization • Vision Analytics & Processing • Optical Character Recognition	• MLOps - Automated ML Pipeline Deployment • Model Designing, Optimization, Testing & Porting • Inference Engines & Metrics • ML Transfer Learning Framework • Data Augmentation & Annotation	• Deep Learning & Neural Networks • AI/ML on Edge & Cloud • ML Application Acceleration • Cross Platform Porting & Integration • Natural Language Processing (NLP)	• Scene Detection & Text Analytics • Predictive Analytics • Audio Analytics & Key-phrase Detection • Face Recognition • ML Reference Designs & POC

AI Tools & Frameworks

Tesseract OCR
TensorFlow
TensorFlow Lite
Keras
spaCy
PyTorch
XILINX VITIS AI
TINY DL
kubernetes
AWS DeepLens
Caffe2
Coral Edge TPU Compiler
LUIS
AutoML
LATTICE sensAI
Azure Machine Learning
amazon Rekognition

Architectures

VGGNet
AlexNet
Inception V3
SqueezeNet
SSD
YOLO
MobileNet v1/v2
ResNet

MULTIMEDIA ENGINEERING

AUDIO SOLUTIONS	VIDEO SOLUTIONS	EMBEDDED & MULTIMEDIA SYSTEMS	CAMERA ENABLED SOLUTIONS	IMMERSIVE SOLUTIONS
• Audio Codec Engineering • Audio Command Detection • Audio Algorithm Development • ALSA Driver Development	• Video Codec Engineering • Surveillance & DVR • Video Analysis & Validation • VoD & Media Streaming • Image Stitching	• Multimedia Framework Integration • Multimedia Systems & SDK Development • Android Multimedia & HAL Development • OpenVX Acceleration • Media Infotainment Systems	• Smart Camera Applications • Firmware & Driver Development • Image Signal Processing (ISP) • Camera Framework Integration	• AR/VR application development • VR gadget feature development • VR streaming on Wi-Fi • Open Standard based VR/AR • VR on Cloud

Audio & Speech Codecs

AAC, DOLBY, dts, MP3, WMA, FLAC

AMR-NB/WB

QCELP

EVRC

Video& Image Codecs

AVI, MPEG

HEVC

H.264

VP8/9

JPG, GIF, PNG

Platforms

NVIDIA, XILINX, LATTICE SEMICONDUCTOR, Texas Instruments, VeriSilicon, CIRRUS LOGIC, QUALCOMM, cadence

Architectures

Multi-core

ARM

DSP

GPUs

Frameworks

FFmpeg, gstreamer, OpenVX, FastCV, STEAMVR, OpenXR, unity, OpenVR

V4L2

Windows Media

OpenMAX IL

DL **DRM**

Streaming & Screen-Casting

Miracast source and sink

RTP | SRTP

Adaptive Streaming Technologies, MPEG2 TS, WebRTC,

Image/Video Analytics

Tiling | Stitching

QUALITY ENGINEERING

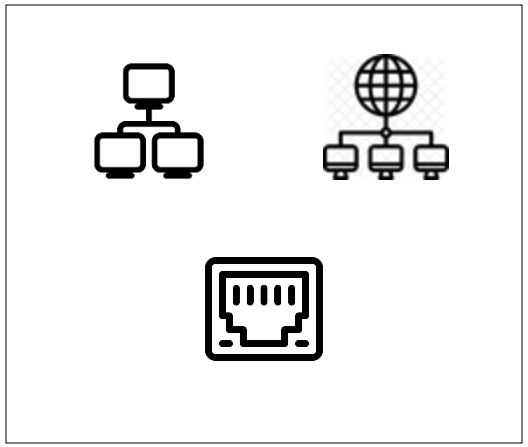
DEVICE & EMBEDDED TESTING	QUALITY ASSURANCE & PRODUCT TESTING	DEVOPS & TEST AUTOMATION	ML TESTING	CERTIFICATION, COMPLIANCE & CONSULTING
• Multimedia, Audio/Video Testing • Embedded System & Integration Testing • Test Tool Development • Network Interface Card Validation • Software Toolchain Testing	• Performance & • Functional Testing • Sensor Integration & Interoperability • Peripherals & Connectivity testing • Connected App/Edge • Testing	• Continuous Integration, Deployment & Testing • Device to Cloud Test Automation • Test Automation Frameworks • Automation Scripts • QA Farms	• Dataset & Feature Validation • Model Validation & Performance • Benchmarking • Model Parameters Traceability • ML Library Integration Testing • Embedded Neural Network Application Testing • CNN Compiler Validation	• FuSa - ISO 26262 • AUTOSAR & MISRA-C • OpenVX Vision Library Conformance • Tools/Frameworks Assessment & Integration Support • Feasibility Analysis • Test Lab Setup Advisory

Automation Frameworks	Test Management	Performance/Load Testing	Version Control	Networking	In-House QA Tool
Jenkins Selenium appium python TestNG Robot Framework	TestRail JIRA TestLink Rational Quality Manager	APACHE JMeter™ LOCUST MONKEY TALK	git TortoiseSVN Bitbucket PERFORCE	WIRESHARK NRF SNIFFER	STAF

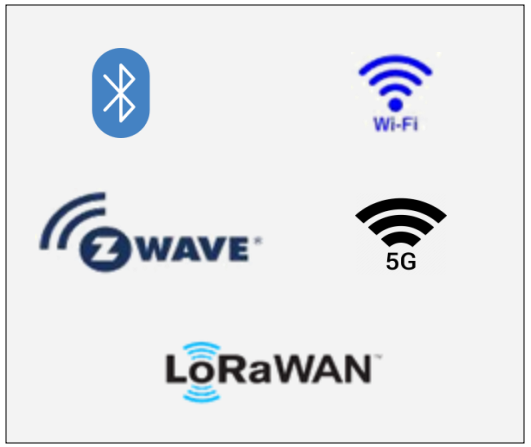
NETWORK ENGINEERING

WIRED	WIRELESS
• Network Protocol & App Development • Network Stack & Performance Optimization • Network Test Automation • Network Module Integration • Software Defined Networking	• Wireless Solutions (Wi-Fi, BLE, RF) • Customer Premise Equipment • WLAN drivers • Wi-Fi co-existence

Wired



Wireless

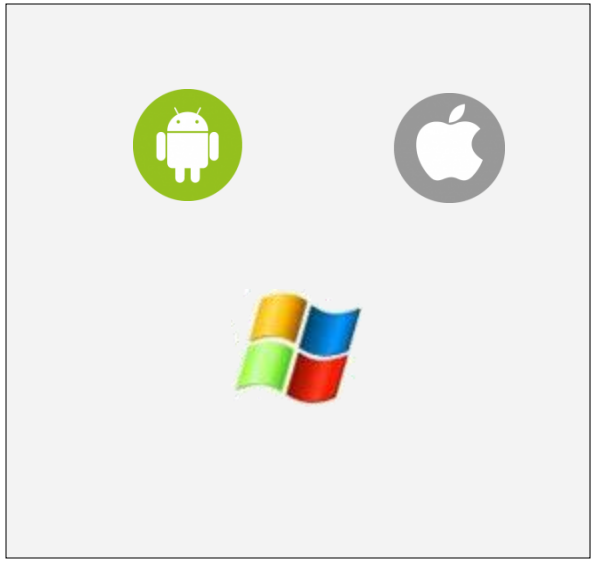


DIGITAL ENGINEERING

IOT	MOBILITY	CLOUD
• IoT Device Connectivity • Gateway Integration & Management • Digital Twin • IoT Device Lifecycle Management • Gateway & Cloud Security	• Mobile App Development • UX Design • Mobile Automation Framework	• Cloud Migration • Cloud Design & Architecture • Cloud Service Integration

Connectivity

Web/ Mobile Applications



Cloud

SUMMARY OF EMBEDDED PROJECTS

Application	Embedded Service
Home Automation	Firmware development of Wi-Fi module
Health Monitoring	Firmware development of Wi-Fi & BLE MCU
Autonomous Driving	ECU software development FuSA (ISO26262), MISRA-C Compliance
Multimedia	GStreamer plugins development & porting
Multimedia	DSP based firmware development, audio codecs driver development
AIML	Data annotation, algorithm training, deployment Computer vision, NLP, OCR, NLP
Multimedia	ALSA compliant Linux kernel audio driver, Audio firmware feature enhancement
Camera	Profile & optimize low level u-boot code, A/V subsystem activation at boot-up, design & develop kernel wrapper module
Inertial Measurement Unit (IMU)	STM firmware development with peripherals like I2C, SPI, USB, etc.
Wireless	BT-Wi-Fi-LTE Co-existence IP firmware development & validation

THANK YOU

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