CORPORATE OVERVIEW 2023

CONNECTING THE WORLD

Silicon | Systems | Software | IoT

OVERVIEW

Established in 1999, with 20+ years of expertise

Developed and shipped millions of connectivity ASICs over the years

Focused on Product Engineering in Mixed signal IP, Turnkey ASICs, Semiconductor and IOT solutions

1300+ engineers spread across Silicon valley - USA, Hyderabad, Bangalore, Ahmedabad & Pune

Domain expertise in IoT, Consumer, Multimedia, Automotive, Networking & Telecommunications, Handheld, Storage, Edge Applications

“We are one of the versatile organizations with solutions & services for almost every industry” - CEO

BUSINESS UNITS

Semiconductors

Semiconductor IP

- Digital IP
- Verification IP
- SerDes IP
- ADC / DAC IP
- PLL IP

Semiconductor Design Services

- RTL design & verification Services
- Analog layout services
- Physical design services

Turn-key ASIC

- RTL to Volume Production
- Working relationship with leading fabs
- Successful track record

Embedded System & Software Design

Product / System Design

- High Speed Product & System Design
- Platform Designs with FPGA, SoC & ASIC's
- DFM / DFA, & EMS
- Platform Bring-up & Validation

Embedded Software

- OS Porting & Board Support Package
- Device Drivers – Bare metal, OS
- Software Integration
- Software Testing
- Software maintenance/ support

ISO 9001:2015 certification for SoC Design, Development, Assembly, Supply & Services of Semiconductors, Software & Systems

LOCATIONS

Global Headquarters

Subsidiary / Branch Office

TECHNOLOGY ALLIANCES

FPGA DESIGN PARTNER	FPGA Microchip Design Partner	Click Here to View Details
CERTIFIED ALLIANCE MEMBER	Xilinx Alliance Program Certified	Click Here to View Details
SENSAI MEMBER	Lattice Semiconductor	Click Here to View Details
BUILD PARTNER	Mentor A Siemens Business	Click Here to View Details

FOUNDRY ALLIANCE – TSMC DCA PARTNER

"We're very pleased with the addition of MosChip to our OIP Design Center Alliance to address the growing market need for design services on TSMC's industry-leading technologies," said **Dan Kochpatcharin**, Head of the Design Infrastructure Management Division at TSMC. "Our partnership with MosChip expands TSMC's design ecosystem and enables our mutual customers to achieve next-generation design success and quickly launch their differentiated products to market."

SEMICONDUCTOR IP

MIXED SIGNAL IP AND RELATED SERVICES

IP → **CUSTOMIZE** → **INTEGRATE**

Mixed-Signal IP

Standards Based IP

- PCIE Gen1/2/3 PHY
- SATA I/2 PHY
- XAUI PHY
- CEI-6G-SR-PHY
- SerialLite PHY & PCS
- ARM HSSTP PHY & Link
- PCIE Gen4 PHY (In Lab)

Analog IP

- ADC, LVDS I/O, PLL

Customer Specific:

- Custom SerDes for automobile / ADC / other applications

- MosChip Technologies offers customization to other Foundries / nodes and emerging standards

Porting to other foundries

  - TSMC, Global, Tower
  - 180nm, 130nm, 55nm 40nm, 28nm, 22nm, 16FF, 14FF, 7FF, 6FF, 4FF, 5FF, 3FF

- MosChip technologies offers design services for customization / porting of customer's own technology

- MosChip Technologies offers complete integration services of their IP into customer's SOCs. In addition, MosChip Technologies' services division provides design services in the following:
- Synthesis
- DFT
- Place & Route
- Analog/Mixed Signal Design
- Analog Layout

ANALOG IP CUSTOMIZATION SERVICES

Nodes		
TSMC	SAMSUNG	GLOBAL FOUNDRY
FinFET 3nm, 5nm, 6nm and 7nm	4nm	12LP
12FFC	5nm	14FF
28nm HPC, HPC+	12nm	22 FDX
40LP, 180nm		40nm, 55nm

CUSTOMER PROJECTS	INTERNAL PLATFORMS
DISPLAY PORT/HDMI SerDes (10G)	Long Range SerDes (16G)
Multi-Protocol SerDes (6.4G)	Short Range SerDes (10G)
DDR4, GDDR5 PHY	ARM HSSTP PHY (12.5G)
TOUCH SENSOR IMAGE SENSOR	ADC
Serial Lite SerDes (2.5G)	LVDS IO, PLL

Design Tools	Layout Tools	Other Tools
cadence	cadence, Mentor Graphics	MATLAB, SOS SYSTEMS, SystemVerilog

50+ Engineers

- Capable of providing Complex IP Porting solutions like Serdes, DDR
- Experience in working with Latest nodes in TSMC and Samsung
- Recognized TSMC Partner (TSMC DCA Partner)
- Adheres to strict IP Development Methodology
- Follows established CAD Flows and Methodology
- Adherence to ISO Standards, ISO9001:2015 Certified Company
- Professional Program Management and Status Updates

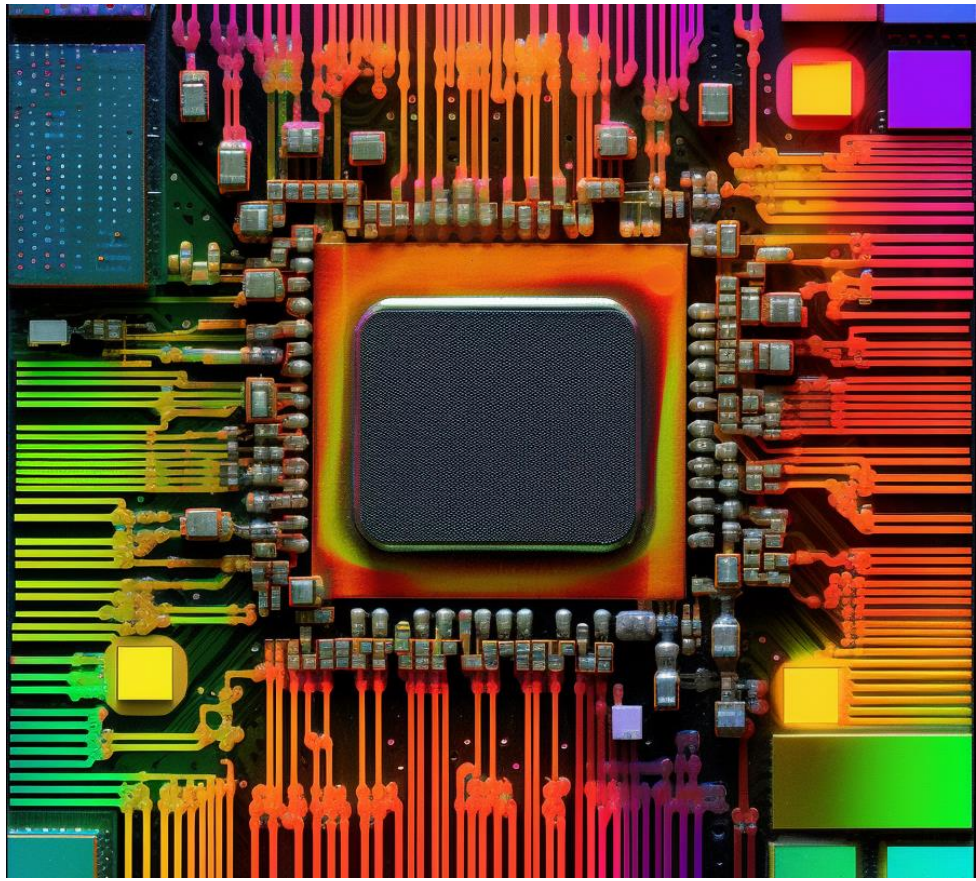
MOSCHIP SERDES IP

[Phy product standards' overview]

Name	Standards	PCS	Data Rate per Lane (Gbps)	Comments
PCIe Gen 1	PCIe 1.1	PIPE	2.5	• Endpoint or Root Complex • PIPE includes skip insertion, deletion • PCIe power savings modes
PCIe Gen 2	PCIe 1.1	PIPE	2.5	• Endpoint or Root Complex • PIPE includes skip insertion, deletion • PCIe power savings modes • Port bifurcation support
	PCIe 2.1	PIPE	5.0	
PCIe Gen 3	PCIe 3.1/2.1/1.1	Partners	8.0	• Endpoint or Root Complex • PCIe standard multi-lane interface
XAUI	XAUI, CX4, KX4	Customer	2.4 - 3.2 / 1.2 - 1.6	• Generic backplane uses
CEI-6	CEI-6, XAUI, CX4, KX4	Customer	4.8 - 6.4 / 2.4 - 3.2 / 1.2 - 1.6	• Generic backplane uses
SATA I/II/III	SATA I/II	SATA	1.5/3.0	• Advanced frequency offset (PPM) compensation for +0 / -0.5% SSC
	SATA III	SATA	6.0	
Switchable	Multiple	Multiple	Multiple	• Switchable between 2 or 3 standards • Separate interface for each standard
ARM HSSTP	HSSTP 6.0	Aurora Link	6.25 / 12.5	• ARM HSSTP PHY along with Link Layer as a single macro
PCIe Gen4	PCIe 4.0	Partners	16	• Test silicon functional and in CHAR/Debug
Seriallite PHY	IEEE149.1	PCS	3.125	• chip2chip, board2board, shelf2shelf or backplane
10/100/1000 Ethernet	IEEE802.3	PCS	1	• AFE Block in development
USR/VSR/SR		PCS	10	• Chip to Chip SerDes. In Development

MOSCHIP DIGITAL IP

USB	SECURITY	ENCRYPTION
• Host Controller • Device Controller • Retimer • Dual-Role-Device	• Secure Hash Algorithms (SHA1, SHA2, SHA3) • Reed-Solomon based FEC • Reed-Solomon based Erasure (Static & Dynamic)	• Advanced Encryption Standard (AES 128, AES 256) • XTS-AES



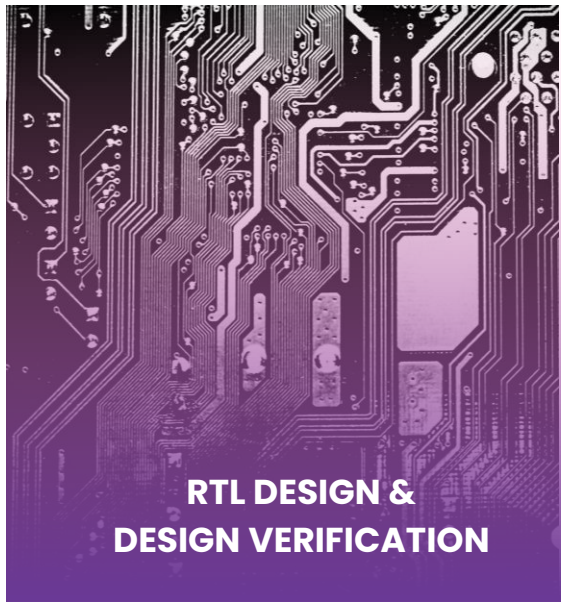
Best in class performance

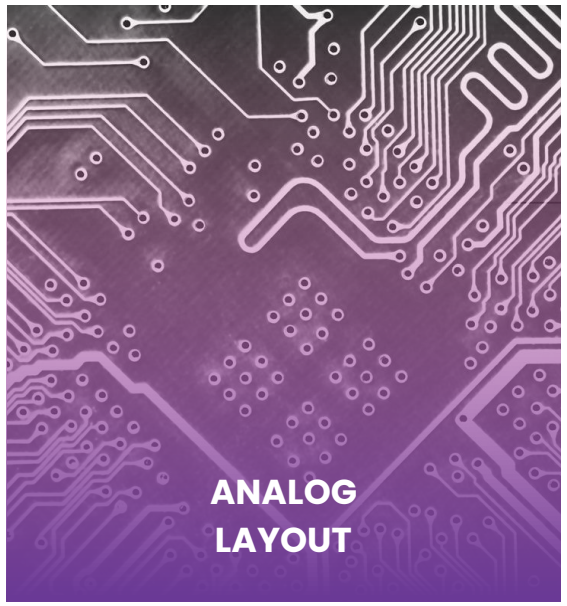
Up to 20% Better throughput

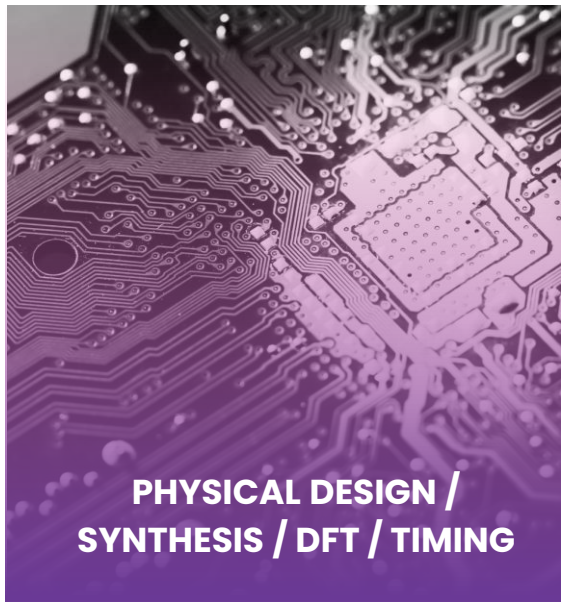
Platform Independent

SEMICONDUCTOR DESIGN SERVICES

OVERVIEW OF SEMICONDUCTOR GROUP







- Achieved "**first-pass silicon success**" across **400+** tape-outs
- Expertise ranging from **500nm** to the latest **3/5/6/7 /10 /14 /16 nm FinFET & SOI process nodes**
- Very strong **RTL Design, Design Verification, Physical Design, Analog Design, and Analog Layout** team with over 15 years of average experience in the senior team
- Engaged in complex chip designs extending to **100+ million gates**
- Highest level of training & experience on state-of-the-art technologies
- Design Houses in **Hyderabad, Bengaluru, Ahmedabad, Pune** and **Santa Clara, USA**

900+ VLSI Engineers

400+ Tape-outs with 100% First-Pass Silicon Success

Engagement Model ODC | T&M | Turnkey

RTL DESIGN & DESIGN VERIFICATION SERVICES

18+
AVG.EXP. OF LEADERSHIP

100+
TAPE-OUTS

200+
ENGINEERS

RTL DESIGN & VERIFICATION

RTL Design	Verification	TurnKey
RTL Front-end Design & Integration	SV/UVM Expertise	Concept to Deployment
Micro-architecture Design	Assertion based Verification	IP to SoC Design & Prototyping
Synthesis & Optimization	Constrained Random & Coverage-driven Verification	Architecture, Coding, Testing, Release & Support
Low power and GLS	IP/SoC level Verification	Functional Verification
IP/VIP Development, 3rd party IP/VIP& SoC integration	IP to SoC Verification Sign-off	

PROCESSOR

arm

RISC-V

tensilica

mali Visual Computing by ARM

TOOLS

cadence SIEMENS

SYNOPSYS XILINX.

ALTERA.

HIGHLIGHTS

- ★ Digital IPs/Subsystem – GCC, and Arite core
- ★ Mixed signaling IPs – Tejas, Brain beats and Borealis
- ★ Turnkey project – Matrix SoC

LANGUAGES

Verilog HDL SystemVerilog UVM OVM

C/C++ python Perl VMM

TECHNOLOGY EXPERTISE

IP Interfaces / Protocols

Ethernet

HDMI | SATA
SAS | CAN
AXI/APB
xHCI | PIPE
UTMI+ULPI
SPI | I2C
Interlaken
MIPI | DP

Verification Tools

Questa | Incisive
VCS | Jasper
QuestaFormal
Xcellium
Simvision
Visualizer
Codelink Verdi
Formality
FormalPro
QuestaSLEC
Conformal

Languages & Methodology

SystemVerilog

UVM

Scripts

python

Perl

.SH

Shell

Prototype Platforms

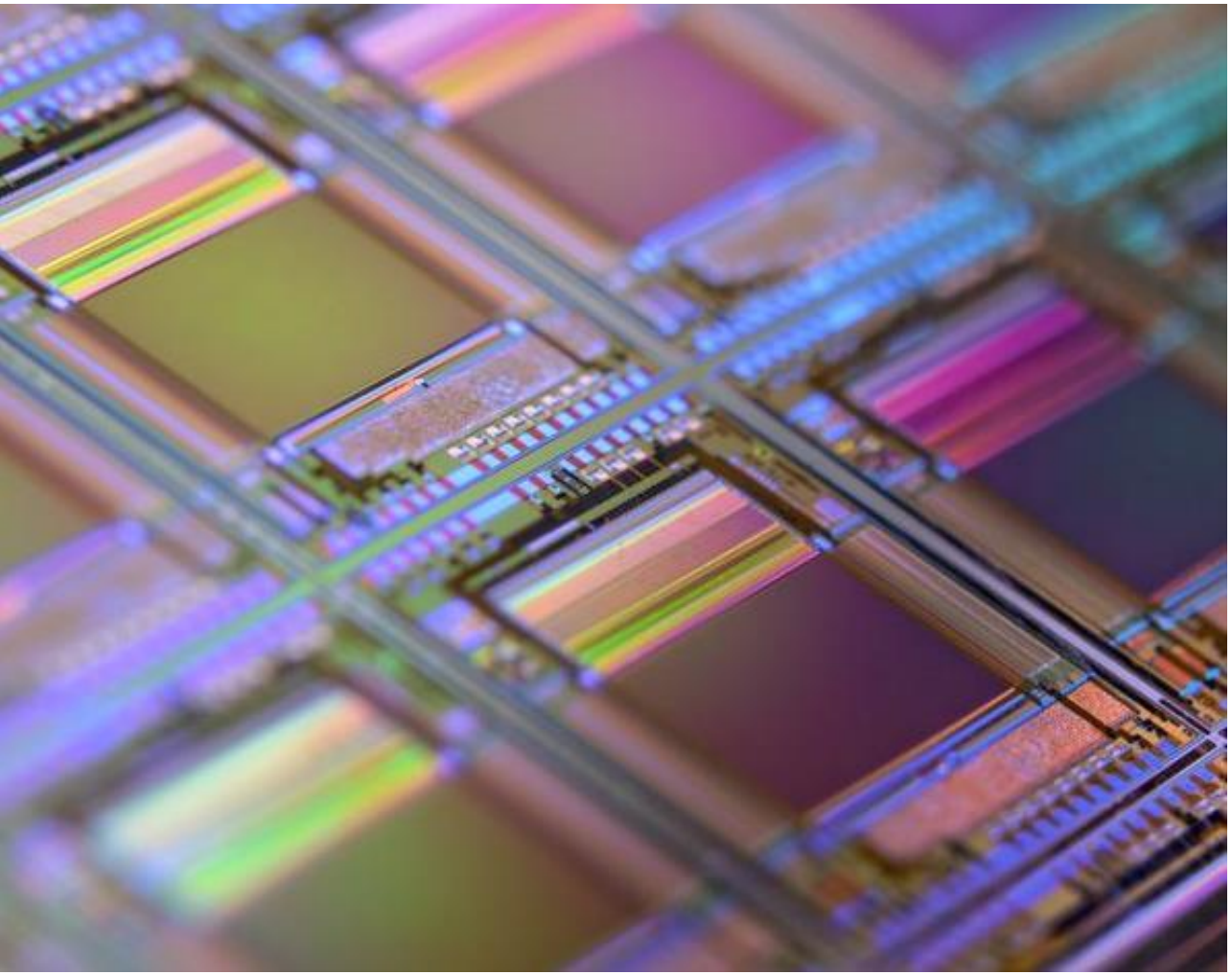
intel

ALTERA
now part of Intel

cadence

XILINX

LATTICE SEMICONDUCTOR



ANALOG LAYOUT SERVICES

18+
AVG.EXP. OF LEADERSHIP

150+
TAPE-OUTS

250+
ENGINEERS

ANALOG LAYOUT SERVICES

Technologies

- TSMC - N3E | N3P | 5FF | 6FF | 7FF | 12FF | 16FF
- TSMC - 22nm, 28nm, 180nm
- SAMSUNG - 3nm, 4nm, 5nm, 7nm
- GF - 14nm, 12nm, 22nm, 40nm, 55nm, 65nm

Expertise

- High Speed Serdes up to 112Gbps – Very Short Reach or Extra Short Reach Serdes of 112Gbps data rate, PCIe6 Gen Protocols
- Power Management Layouts – LDO, BGR, SMPS, Bias blocks, Buck Boost converters, etc.
- I/O cells – GPIOs, LVDS, DDR Ios and GDDR IOs
- Data Converters – ADC, DAC with different architectures (Pipeline, SAR ADC, Flash ADC, Current steering DAC and R-2R ladder DAC)
- RF Layouts
- Memory Layouts – Register files, Dense RAM, Cache Memory, CAM Memory
- Clock Generators – Phase Locked Loop, Delay Locked Loop

UNVEILING

- ★ Ready to Tape-out the Chip in 3nm
- ★ TSMC 22nm Ultra Low Leakage (ULL) AIoT Edge AI SoC for NTU, ASTAR & EMass.ai [RTL-Silicon]

TOOLS

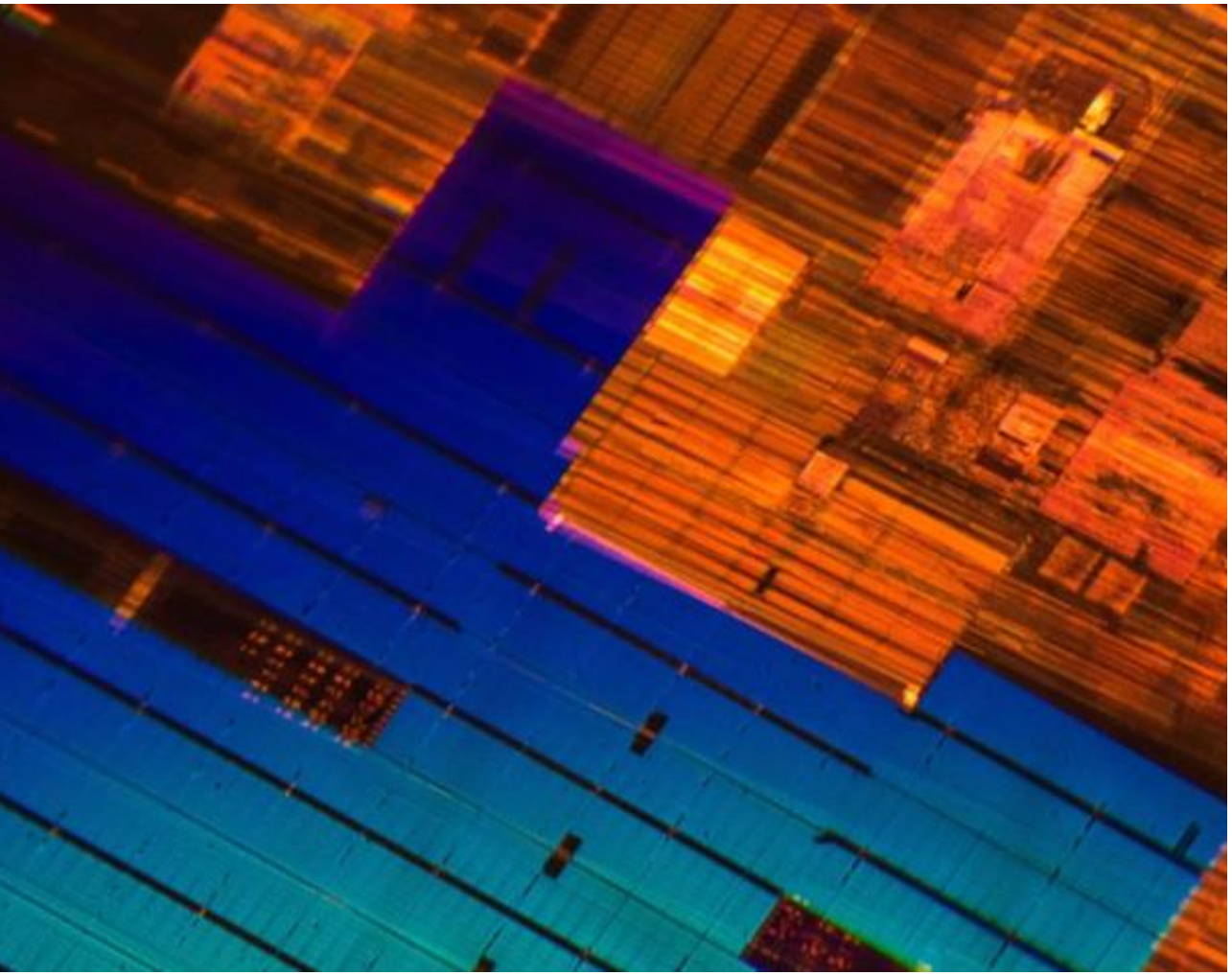
cadence® Mentor Graphics®
Ansys SYNOPSYS®

HIGHLIGHTS

- ★ SerDes - Up-to 112GBPS
- ★ SerDes - PCLe5 & PCLe4 with Multiprotocol support
- ★ SerDes - Up-to 112GBPS

ANALOG LAYOUT – IP DETAILS

PRODUCT	TECHNOLOGY	SPECIFICATION	APPLICATION
XSR SerDes	TSMC N5	112 Gbps	Networking/Servers
PCIe Gen6	TSMC N5	64 Gbps	Networking / Servers
DDRIO	TSMC N3	4.8 Gbps - 5.6 Gbps	Memory Applications
DDRIO	TSMC 5G	4.8 Gbps - 5.6 Gbps	Memory Applications
DDRIO	Samsung 5nm	4.8 Gbps - 5.6 Gbps	Memory Applications
Graphical DDR	TSMC 12FFC	12 Gbps	Memory Applications
PMU / PMW Controllers	TSMC180		Laptop / Servers
High Precision Oscillators	TSMC N55	Speed of 5Ghz	Aerospace, Defense, Automotive, Electronics, Mobile & IoT
Clock Generator	TSMC N3	Speed of 5Ghz	Processors
Smart Electrical Meter IC	TSMC 180	45-55Hz, 1 Phase / 3 Phase	Electric Measuring Applications



PHYSICAL DESIGN SERVICES

20+
AVG.EXP. OF LEADERSHIP

150+
TAPE-OUTS

400+
ENGINEERS

PHYSICAL DESIGN SERVICES

EXPERTISE

- Block-Level Place & route
- Timing Closure & Static Timing Analysis
- Multiple Domain Clock-Tree Synthesis
- Physical Verification (DRC/ERC/LVS)
- EM-IR Drop Analysis, SI Closure
- Chip-Integration
- Logic Synthesis & Physical Synthesis
- Low Power Expertise – Clock Gating, Multi-Vt, Voltage Islands, Power Gating

FLIP-CHIP EXPERTISE

- O-ring design
- Bump Assignment work with Package team and Finalize
- Customer Designed Bump/RDL integration to chip level
- RDL Design and Routing
- Help Customers to decide Metal Stack
- Bumps and Package

TECHNOLOGIES

tsmc
GlobalFoundries
SAMSUNG SEMICONDUCTORS
Tower Semiconductor

LEADERSHIP HISTORY

ttm Time To Market Inc.
GigaCom
FIRSTPASS Committed to customer success
MOSCHIP

HIGHLIGHTS

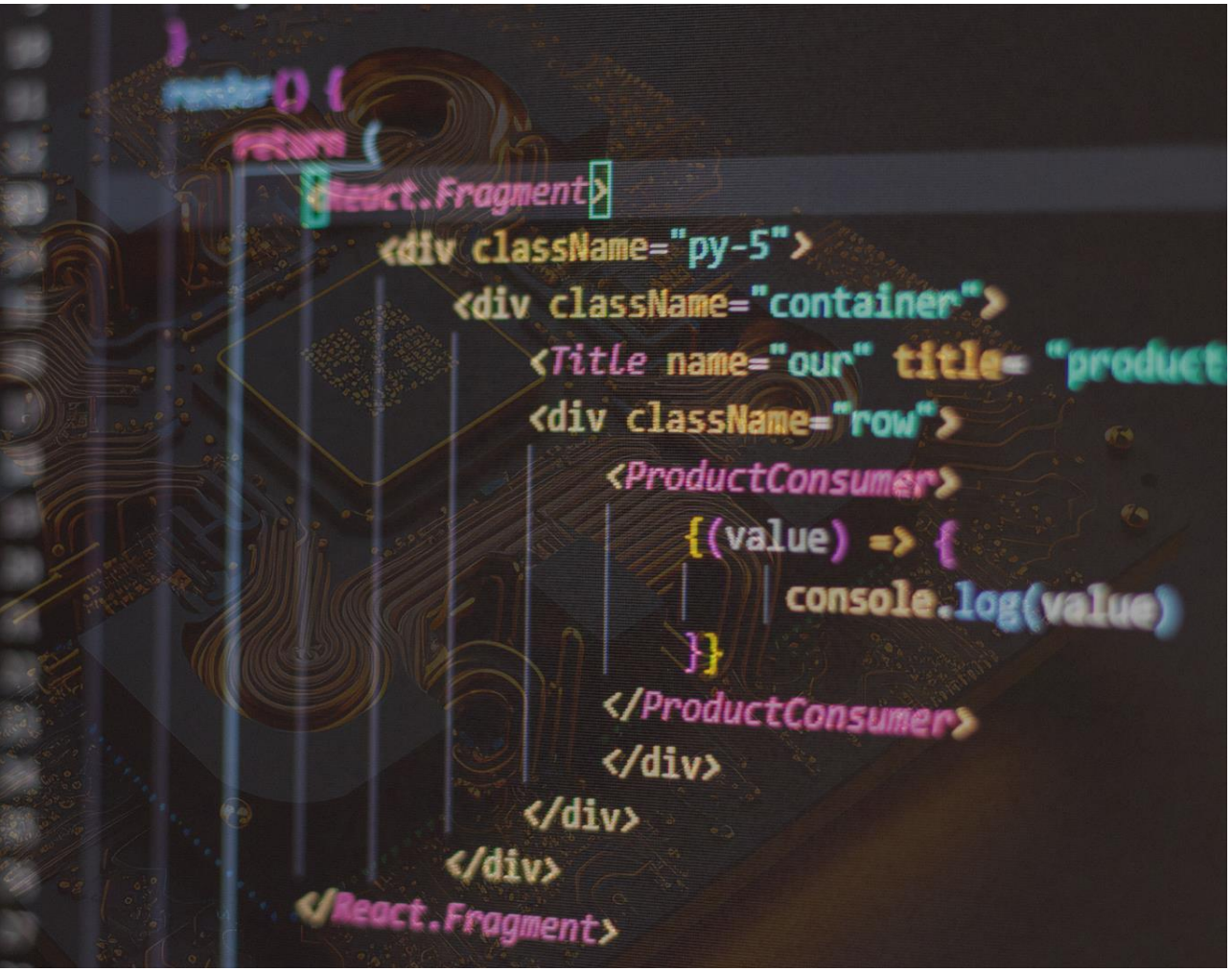
- Full-Chip Integration | Floor-Plan | Analog Integration | IP-Integration
- Full-Chip Pin-Assignment & Budgeting | Power-Grid Design & Analysis
- Clock-Design | timing Closure | Physical Verification & EM-IR
- DDR-Integration using new generation timing libraries (LVF)

TOOLS

cadence
SIEMENS
SYNOPSYS
Mentor Graphics

SUMMARY OF RECENT & RELEVANT SAMPLE PD PROJECTS

PROCESS	APPLICATION	DESIGN FEATURES	TEAM SIZE PD ENGINEERS	FLOW	DURATION MONTHS	STATUS
TSMC 5nm	Client SoC	~ 75M gates, ~ 30 Blocks	15	Customer	12	In Progress
TSMC 6nm	Client SoC	~ 190M gates, ~ 66 Blocks	35	Customer	12	Taped-out
TSMC 6nm	Client SoC	~ 70M gates, 20 Blocks	15	Customer	7	Taped-out
TSMC 6nm	GPU	~ 365M gates, ~ 100 Blocks	50	Customer	11	In Progress
TSMC 7nm	GPU	~ 275Mgates, ~ 80 Blocks	44	Customer	12	Functional
TSMC 16nmFFP	Video Game	~ 22M gates, 25 Blocks	10	Customer	10	Production
GF 14LLP	Graphics	~ 40M gates, 30 blocks	11	Customer	12	Production
TSMC 28nm HPC+	Networking	~ 103M gates, 14 Blocks	12	MosChip	15	Production
TSMC 40nm G	Networking	~ 12M gates, 8 Blocks	8	MosChip	7	Production
GF 14nm HPP	Ethernet	~ 28M gates, 9 Blocks	6	MosChip	7	Production
TSMC 28nm HPC+	GSP	~ 93M gates, 3 (Unique) Blocks	6	MosChip	12	Functional (PoC)
Samsung 14nmLPP	GSP	~ 120M gates, 3 (Unique) Blocks	6	MosChip	12	Production
TSMC 22nm ULL	Edge SoC	~ 2.2M gates, Flat Chip	3	MosChip	4	Bring-up



EMBEDDED SYSTEMS, SOFTWARE & PRODUCT DESIGN SERVICES

OVERVIEW OF EMBEDDED GROUP

MosChip offers various Embedded Product Design Services such as:

- **Embedded Product Design:**
  - Turn-key solutions with System Design, Software Development, FPGA Integration, Bring-up, Validation & Manufacturing / Production Enablement & Improvements, Formfactor Designs for Custom or COTS Enclosures
- **Embedded System Software Development:**
  - BSP / OS Porting, Device Drivers, Integration, Bring-up, Validation & Maintenance with Version Control
- **Complex & High-Speed System Design:**
  - System Architecture / Schematic Design, PCB Layout, SI / PI / Thermal Sims, Bring-up, Validation, Design updates with Version Control, Prototyping and Manufacturing

OS PORTING & BOARD SUPPORT PACKAGE (BSP)	
PROCESSORS	

400+ Engineers

- 23+ Years Track Record with 500+ projects in Embedded Software Development & System Design
- Enabling solutions from Concept > POC > Production > Field Enablement
- Flexible engagement models in catering to Semiconductors, Defence, Medical, Storage, Computing, Consumer & IoT Product Segments
- Proven workflow of multiple designs with different Clients at different geo-graphic locations & product segments
- Engineering Partners for Indian Defence Labs

MULTIMEDIA	Display / Video / Audio Codecs & Controllers HDMI, MIPI, CSI, DSI, Touch Screen, LCD/LVDS
PERIPHERALS	DMA, I2C, I2S, McBSP, UART, MMC/SD, SPI, eMMC, SDIO, NAND, NOR, DDR3/DDR4, PMIC & Power Management
CONNECTIVITY	USB, PCI/PCIe, WLAN, IrDA ,Ethernet, ZigBee, BT/BLE, GPS, NFC

EMBEDDED SOFTWARE – SKILL SUMMARY

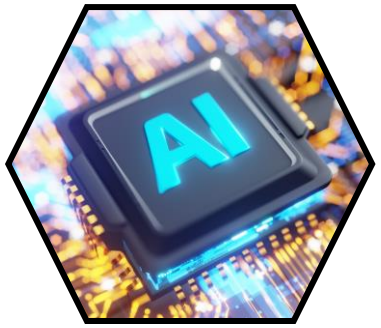
APPLICATIONS	• GUI Design for Si Bring-up / Validation, Configuration & Diagnostics • Custom Applications – USB Over Ethernet, Serial Over Ethernet, NAS etc., • Low Level Firmware and Post
MIDDLE WARE	• Multimedia – Display, Audio / Video Codecs & Controllers, HDMI, MIPI – CSI / DSI, Touch Screen, LCD/LVDS • Power Management • Connectivity - BT, WIFI, NFC, Zigbee & GPS / GNSS
SYSTEM SOFTWARE	• PBL, Uboot, XBL (UEFI), POST • BSP, Board Bring-up • Kernel & Device Drivers (I2C, I2S, UART, MMC/SD, SPI, eMMC, SDIO, NAND, NOR, DDR, USB, PCI/PCIe, WLAN, Ethernet)
OPERATING SYSTEMS	• Linux • Android • Windows • RTOS – Vx Works, FreeRTOS • Lattice SenseAI • Arm Mbed
PLATFORMS	• ARM, Freescale, TI, Samsung, Qualcomm, Xilinx, Lattice. Broadcom, Intel, Microchip Processors

EMBEDDED SOFTWARE CAPABILITIES

Platform Engineering

Multimedia Engineering

Digital Engineering



AI Engineering

Quality Engineering

Network Engineering

PLATFORM ENGINEERING

FPGA DESIGN	EMBEDDED SYSTEMS & SOFTWARE DEVELOPMENT	SECURITY
• RTL Front-End Design & Integration • FPGA Software & Systems Bring-up • FPGA Acceleration Solutions • Interface & IP Integration • Reference Design	• Platform Enablement • Firmware & Driver Development • BSP & Board Bring-up OS Porting & Bootloader Optimization • Middleware Integration • Product Re-Engineering & Sustenance	• Secure Platform Root-of-Trust (PRoT) • Fuzz & Penetration Testing • Edge to Cloud Security • Device & Data Security Lifecycle Management • Identity & Access Management

Device Tools & Frameworks

yocto PROJECT
Code Composer Studio
XILINX VITIS
LDRA
LATTICE sensAI
Auvid
LATTICE RADIANT
IAR Embedded Workbench
OpenWrt
PyCharm
Audacity

Operating Systems

LATTICE sensAI
Linux
android
ARMmbed
VxWorks
Custom Linux

Edge Tools & Frameworks

docker
AWS IoT
LDRA
WIRESHARK
ZAP
Azure Edge IoT Services
metasploit
coverity
Nessus vulnerability scanner
KALI LINUX
EDGE X FOUNDRY
MISRA
USB Analyzer
BLE Protocol Analyzer

AI ENGINEERING

COMPUTER VISION	ML LIFECYCLE MANAGEMENT	COGNITIVE COMPUTING	AI/FPGA ACCELERATION SOLUTIONS
• Machine & Computer Vision Algorithms • Object Detection, Identification & Visual Perception • Image Capture & Optimization • Vision Analytics & Processing • Optical Character Recognition	• MLOps - Automated ML Pipeline Deployment • Model Designing, Optimization, Testing & Porting • Inference Engines & Metrics • ML Transfer Learning Framework • Data Augmentation & Annotation	• Deep Learning & Neural Networks • AI/ML on Edge & Cloud • ML Application Acceleration • Cross Platform Porting & Integration • Natural Language Processing (NLP)	• Scene Detection & Text Analytics • Predictive Analytics • Audio Analytics & Key-phrase Detection • Face Recognition • ML Reference Designs & POC

AI Tools & Frameworks

Architectures

VGGNet
AlexNet
Inception V3
SqueezeNet
SSD
YOLO
MobileNet v1/v2
ResNet

MULTIMEDIA ENGINEERING

AUDIO SOLUTIONS	VIDEO SOLUTIONS	EMBEDDED & MULTIMEDIA SYSTEMS	CAMERA ENABLED SOLUTIONS	IMMERSIVE SOLUTIONS
• Audio Codec Engineering • Audio Command Detection • Audio Algorithm Development • ALSA Driver Development	• Video Codec Engineering • Surveillance & DVR • Video Analysis & Validation • VoD & Media Streaming • Image Stitching	• Multimedia Framework Integration • Multimedia Systems & SDK Development • Android Multimedia & HAL Development • OpenVX Acceleration • Media Infotainment Systems	• Smart Camera Applications • Firmware & Driver Development • Image Signal Processing (ISP) • Camera Framework Integration	• AR/VR application development • VR gadget feature development • VR streaming on Wi-Fi • Open Standard based VR/AR • VR on Cloud

Audio & Speech Codecs

AAC, DOLBY, dts, MP3, WMA, FLAC

AMR-NB/WB

QCELP

EVRC

Video& Image Codecs

AVI, MPEG

HEVC

H.264

VP8/9

JPG, GIF, PNG

Platforms

NVIDIA, XILINX, LATTICE SEMICONDUCTOR, Texas Instruments, VeriSilicon, CIRRUS LOGIC, QUALCOMM, cadence

Architectures

Multi-core

ARM

DSP

GPUs

Frameworks

FFmpeg, gstreamer, OpenVX, FastCV, STEAMVR, OpenXR, unity, OpenVR, OpenVR, V4L2, Windows Media, OpenMAX IL, DL, DRM

Streaming & Screen-Casting

Miracast source and sink

RTP | SRTP

Adaptive Streaming Technologies,

MPEG2 TS, WebRTC,

Image/Video Analytics

Tiling | Stitching

QUALITY ENGINEERING

DEVICE & EMBEDDED TESTING	QUALITY ASSURANCE & PRODUCT TESTING	DEVOPS & TEST AUTOMATION	ML TESTING	CERTIFICATION, COMPLIANCE & CONSULTING
• Multimedia, Audio/Video Testing • Embedded System & Integration Testing • Test Tool Development • Network Interface Card Validation • Software Toolchain Testing	• Performance & • Functional Testing • Sensor Integration & Interoperability • Peripherals & Connectivity testing • Connected App/Edge Testing	• Continuous Integration, Deployment & Testing • Device to Cloud Test Automation • Test Automation Frameworks • Automation Scripts • QA Farms	• Dataset & Feature Validation • Model Validation & Performance Benchmarking • Model Parameters Traceability • ML Library Integration Testing • Embedded Neural Network Application Testing • CNN Compiler Validation	• FuSa - ISO 26262 • AUTOSAR & MISRA-C • OpenVX Vision Library Conformance • Tools/Frameworks Assessment & Integration Support • Feasibility Analysis • Test Lab Setup Advisory

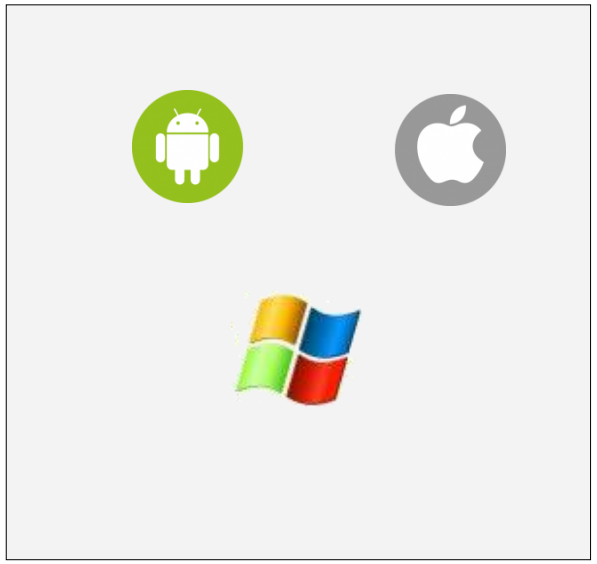
Automation Frameworks	Test Management	Performance/Load Testing	Version Control	Networking	In-House QA Tool
Jenkins Selenium appium python TestNG Robot Framework	TestRail JIRA TestLink Rational Quality Manager	APACHE JMeter™ LOCUST MONKEY TALK	git TortoiseSVN Bitbucket PERFORCE	WIRESHARK NRF SNIFFER	STAF

DIGITAL ENGINEERING

IOT	MOBILITY	CLOUD
• IoT Device Connectivity • Gateway Integration & Management • Digital Twin • IoT Device Lifecycle Management • Gateway & Cloud Security	• Mobile App Development • UX Design • Mobile Test Automation Framework	• Cloud Migration • Cloud Design & Architecture • Cloud Service Integration

Connectivity

Web/ Mobile Applications

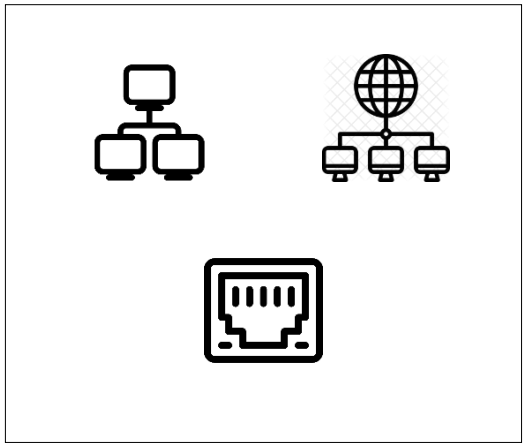


Cloud

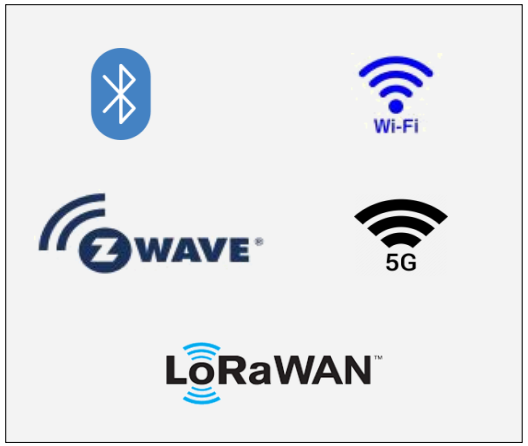
NETWORK ENGINEERING

WIRED	WIRELESS
• Network Protocol & App Development • Network Stack & Performance Optimization • Network Test Automation • Network Module Integration • Software Defined Networking	• Wireless Solutions (Wi-Fi, BLE, RF) • Customer Premise Equipment • WLAN Drivers • Wi-Fi Co-existence

Wired

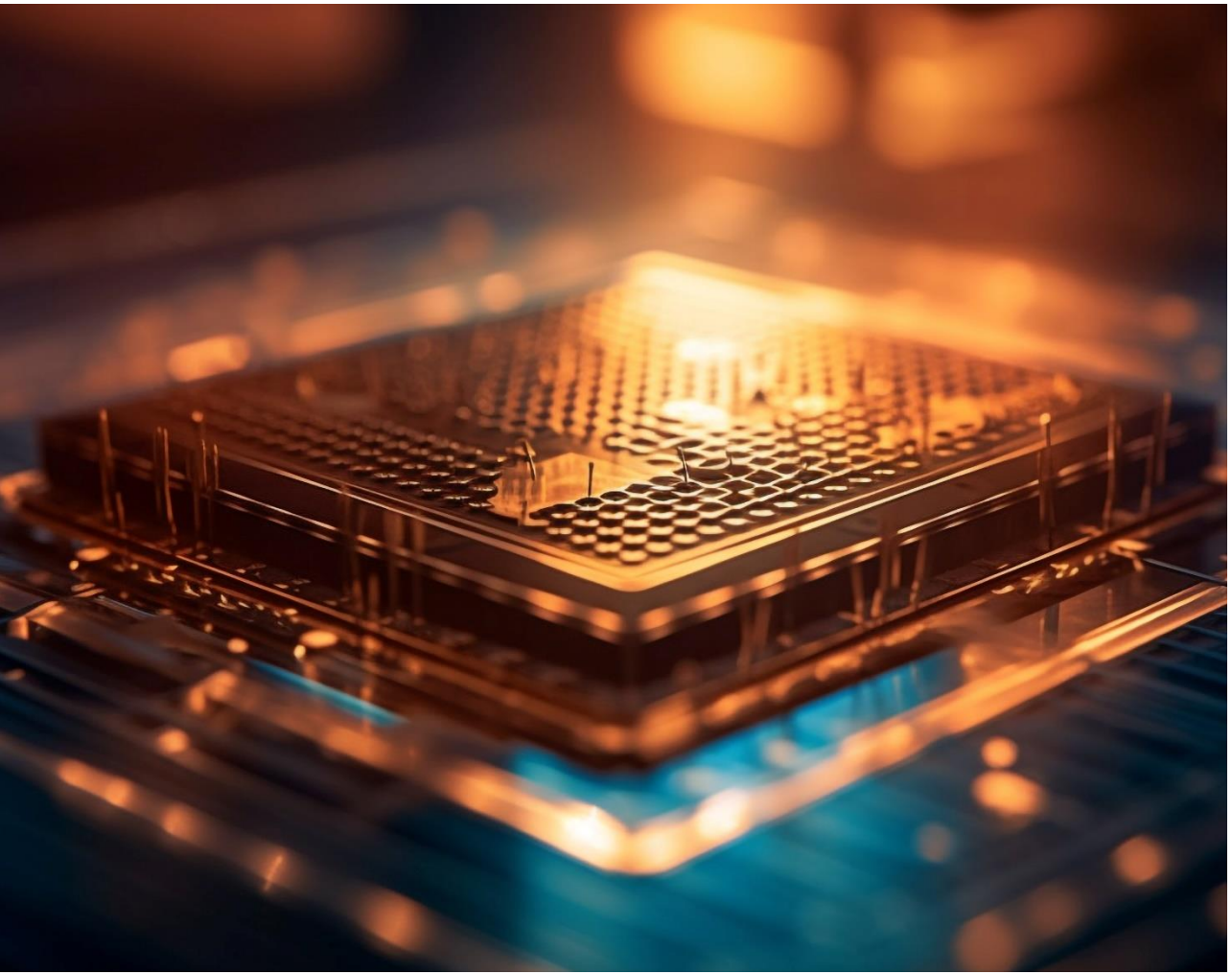


Wireless



SUMMARY OF RELEVANT SAMPLE EMBEDDED PROJECTS

Application	Embedded Service	Status
Home Automation	Firmware development of Wi-Fi module	Completed
Health Monitoring	Firmware development of Wi-Fi & BLE MCU	Completed
Autonomous Driving	ECU software development FuSA (ISO26262), MISRA-C Compliance	Completed
Multimedia	GStreamer plugins development & porting	Completed
Multimedia	DSP based firmware development, audio codecs driver development	Completed
AIML	Data annotation, algorithm training, deployment Computer vision, NLP, OCR, NLP	Completed
Multimedia	ALSA compliant Linux kernel audio driver, Audio firmware feature enhancement	Completed
Camera	Profile & optimize low level u-boot code, A/V subsystem activation at boot-up, design & develop kernel wrapper module	Completed
Inertial Measurement Unit (IMU)	STM firmware development with peripherals like I2C, SPI, USB, etc.	Completed
Wireless	BT-Wi-Fi-LTE Co-existence IP firmware development & validation	Completed



SEMCIONDUCTOR TURNKEY ASIC

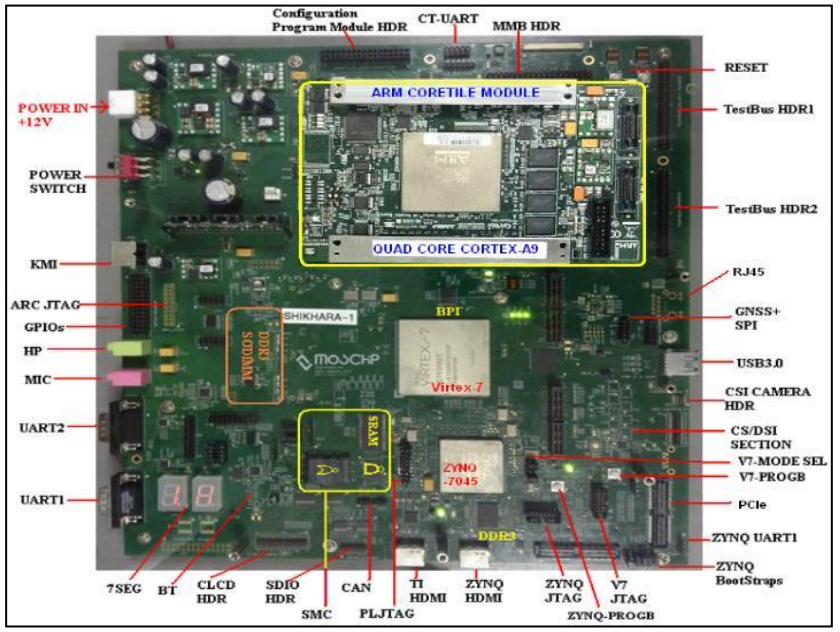
[RTL TO VOLUME PRODUCTION AND BRING-UP]

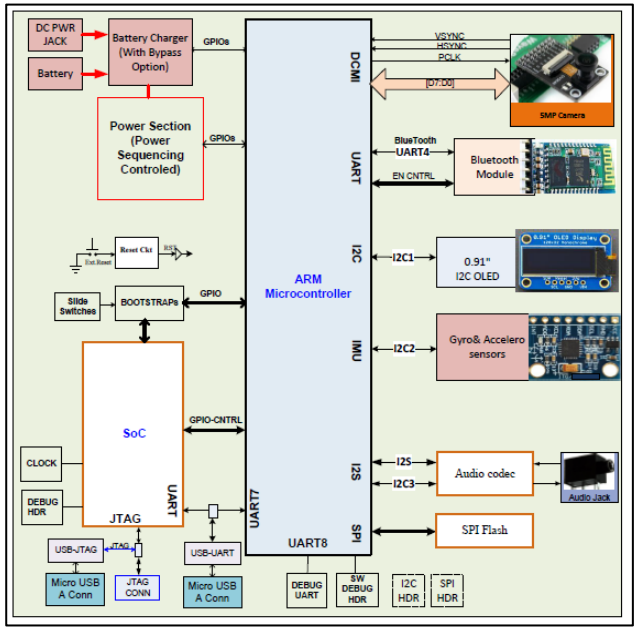
TURNKEY ASIC ECO PARTNERS

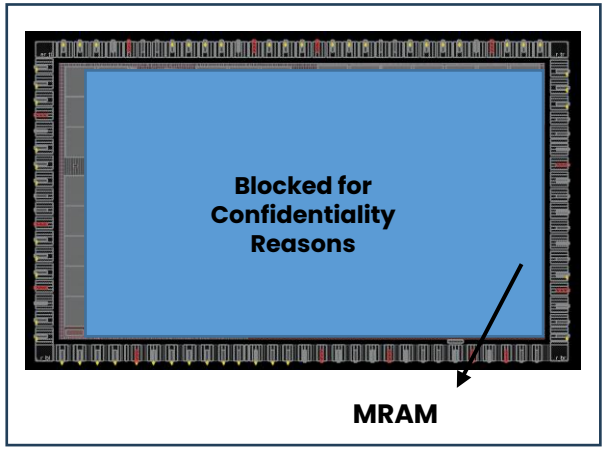
RTL to Volume Production

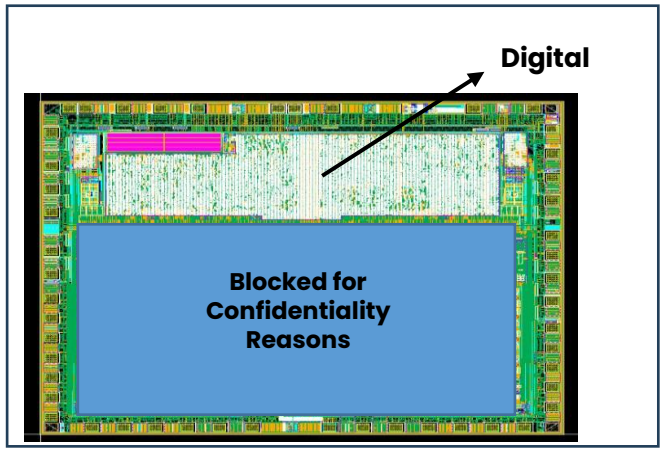
TURNKEY ASIC

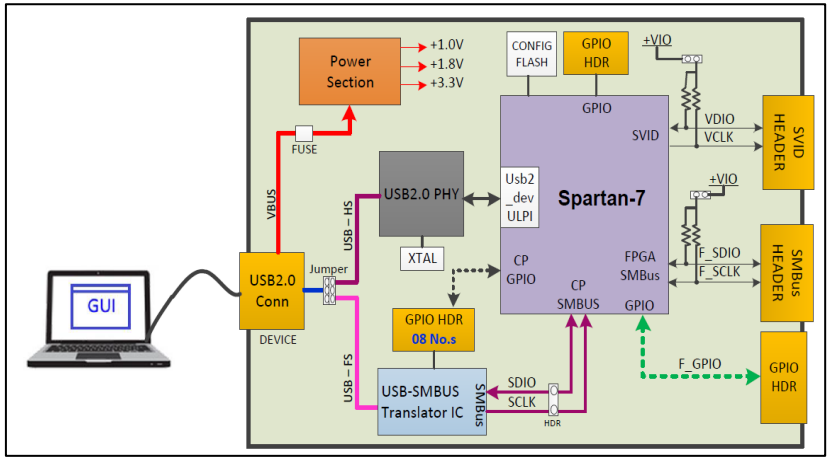
- Turnkey ASIC – Edge SoC
- Turnkey Mixed Signal ASIC – POWER IC
- Edge SoC Reference Platform & Bring-up
- Power IC - Debug Platform Development
- Turnkey ASIC – Matrix (Digital SoC)
- Matrix - FPGA Platform Pre-Silicon Validation
- Matrix – Reference Platform & BSP

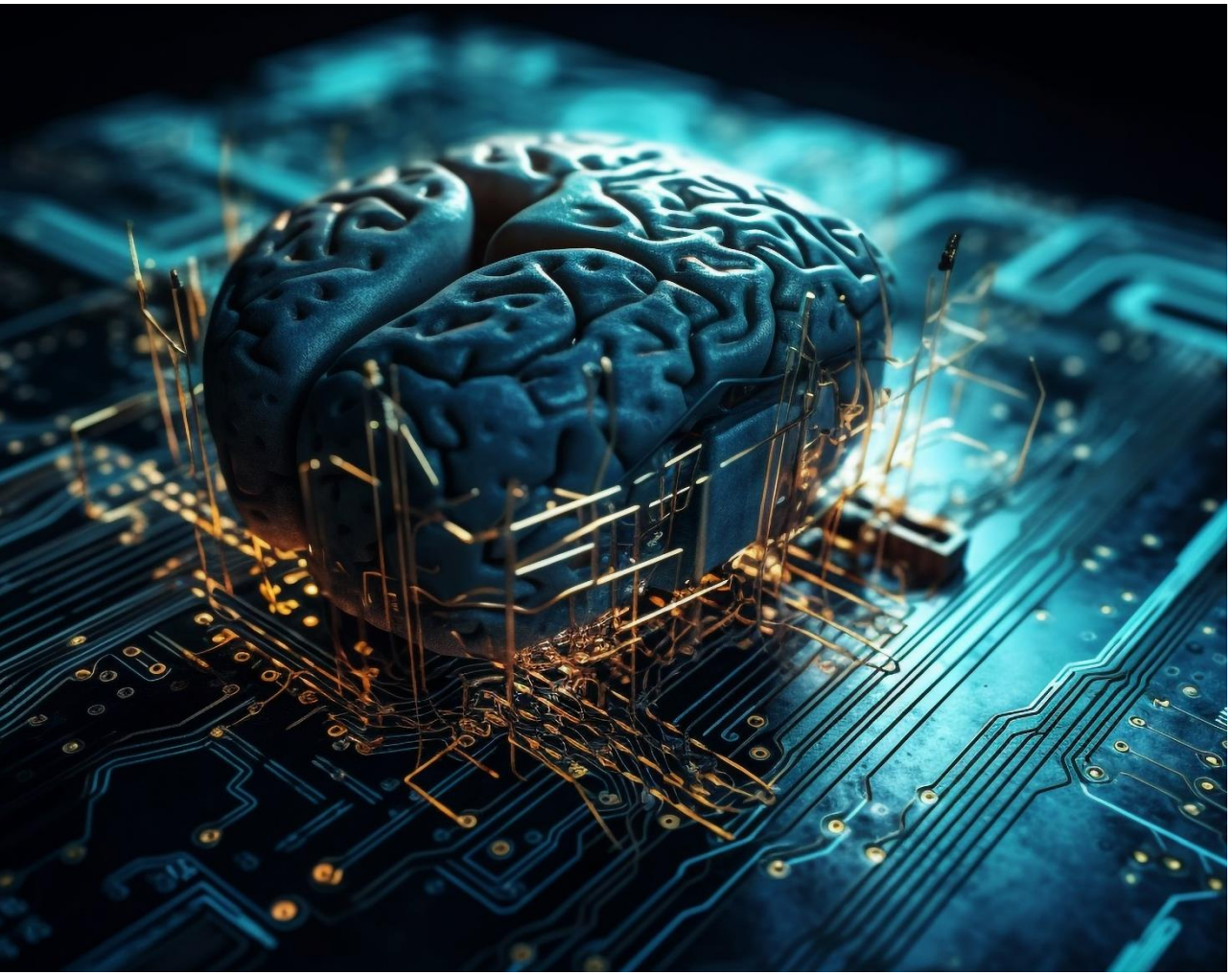








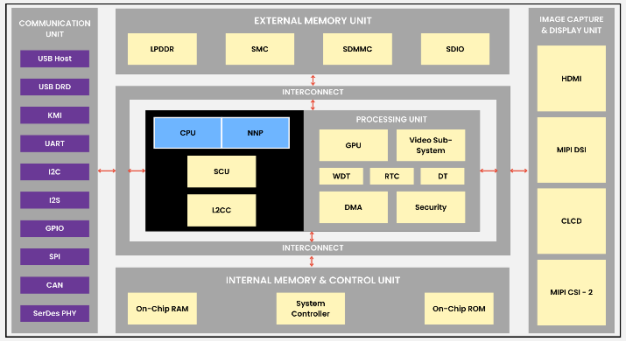




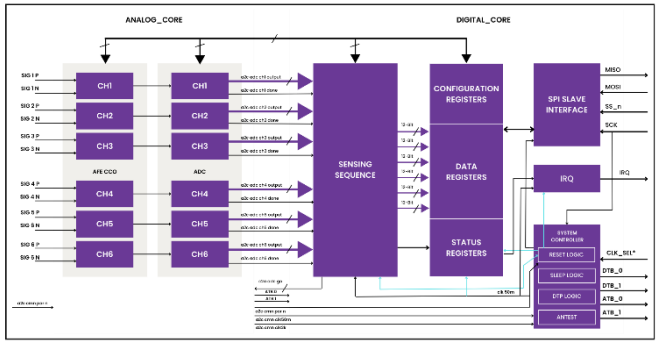
MosChip
ASIC PLATFORMS

MOSCHIP ASIC PLATFORMS

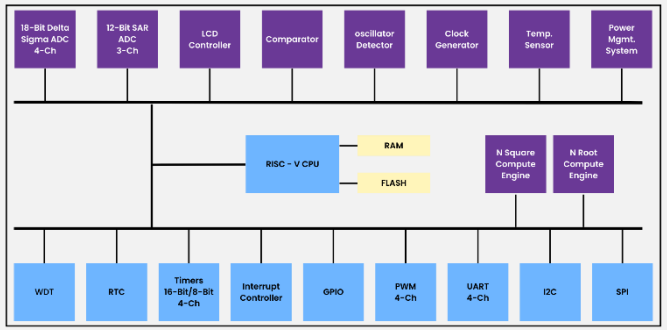
NNP BASED ASIC PLATFORM FOR EDGE AI



LOW FREQUENCY MONITORING ASIC PLATFORM FOR HEALTHCARE



RISC-V BASED ASIC PLATFORM FOR SMART METERS



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