Date: 14th October, 2021

To
General Manager - Listing
The Department of Corporate Services – CRD
BSE Ltd,
PJ Towers, Dalal Street,
Mumbai – 400 001.

Dear Sir/Madam,

Sub: Submission of a copy of press release

Ref: Scrip Code: 532407

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With reference to the subject cited above, please find attached a copy of the press release on Business Update being issued to press/media.

Kindly take the above information on your records.

Thanking you,

Yours faithfully,
For MosChip Technologies Limited,

CS Suresh Bachalakura
Company Secretary

MOSCHIP ANNOUNCES MULTI-PROTOCOL LONG RANGE 8G SERDES PHY in 28nm

Supporting PCIe Gen3.1, XAUI, CEI, SATA3, KX4, Display Port, MIPI M-PHY Standards

MosChip Technologies Limited, a semiconductor and system design services company, unveils today, multi-protocol Long Range (LR) 8G SerDes PHY in 28nm. MosChip has over a twenty-year track record in designing semiconductor IP, products, and SoCs for IoT, networking, industrial, and consumer applications.

MosChip was the first fabless semiconductor company out of India and developed many connectivity-based products that were fabricated at leading foundries and shipped in millions of units. With the acquisition of Gigacom in 2018 the company has developed niche expertise in the areas of analog, mixed-signal design, high-speed serial interfaces, and IP portfolio which includes silicon proven SerDes, PLLs, and Data converters. The multi-lane multi-protocol LR 8G PHY IP is part of MosChips' high-performance multi-rate transceiver portfolio, meeting the growing needs for small footprint, low-power consumption and low latency edge applications.

"Our LR 8G PHY is implemented as a self-contained protocol-agnostic Physical Medium Attachment (PMA) IP with a flexible digital I/ F on the system side that could be made compatible with the most PCS standard definitions that exist in the industry today" said Albert Vareljian, Chief Architect at MosChip. " PHY is based on our innovative self-tuning architecture and fully adaptive continuous-time equalizer with automatic gain control analog front end (AFE) combined with adaptive multi-tap decision feedback equalization (DFE) to cover channel variations and PVT ".

PHY is fully configurable for programmable lane enable/ disable and choice of macros pre-configured for 1 to 16 lanes and supports various debug features such as serial and parallel loop back. The 8G PHY macro is backward compatible and can operate in compliance to PCI Gen1/ 2, SATA 1/ 2 specifications. It includes a PCIe standard multi-lane interface. No external passive components required, saving area at the system level and pin count at the chip level.

"This is a major milestone for MosChip, which highlights our strategic focus to develop niche SerDes PHY IP that is customizable as per customer end applications," said Venkata Simhadri, MD/ CEO of MosChip. With the addition of silicon proven LR 8G PHY to our portfolio, we are well positioned to provide both custom/ porting PHY IP services and turn-key mixed-signal ASIC solutions.

LR 8G PHY macro deliverables include a complete set of logical views, physical views, and documentation, including a Verilog model, a UVM-based verification environment, abstract view, liberty files, GDS-II, netlist and flip chip bump maps.

About MosChip

MosChip Technologies Limited is a publicly-traded semiconductor and system design services company headquartered in Hyderabad, India, with 600+ engineers located in silicon valley-USA, Hyderabad, and Bangalore. MosChip provides turn-key digital and mixed-signal ASICs, design services, SerDes IP, and embedded system design solutions. Over the past 2 decades, MosChip has developed and shipped millions of connectivity ICs. For more information, visit www.moschip.com.

SAFE HARBOR: This release comprises certain forward-looking statements that involve risks and uncertainties. Our actual results could differ materially from those mentioned in such forward-looking statements. The financial impact of this new technology cannot be directly measured.

The risks and uncertainties including but not limited to, those risks and uncertainties, viz, our ability to compete in highly competitive semiconductor industry, ability to define, develop and sell new products, dependency on subcontractors for the supply and quality of raw material, dependency on markets considering the cyclical nature of the industry and our ability to attract and retain technical manpower. MosChip may from time to time make additional forward-looking statements in any manner and does not undertake to update any of these forward-looking statements that may be made from time to time by or on behalf of the company.